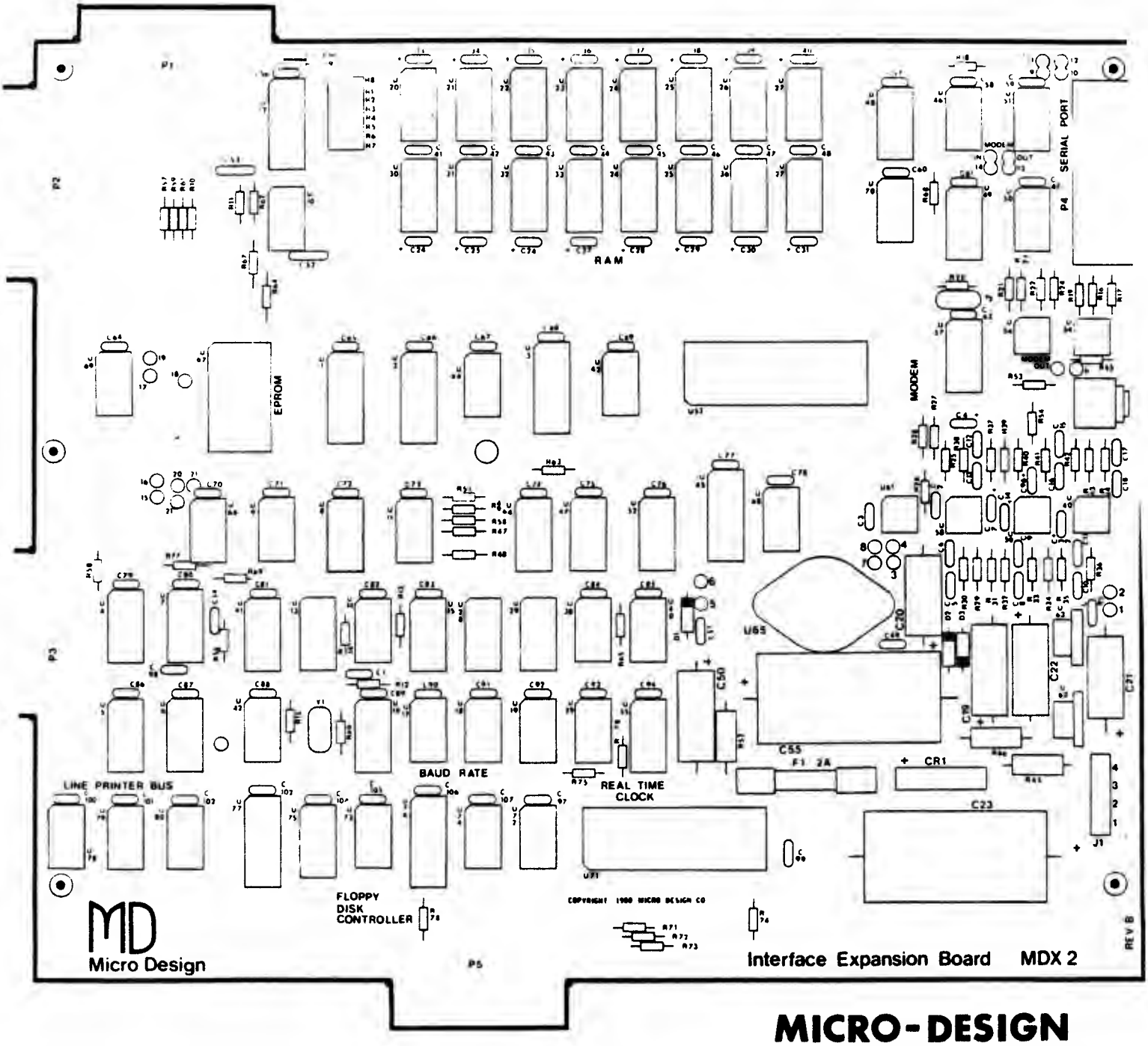
MDX-2

INTERFACE EXPANSION BOARD



MICRO-DESIGN
Austin, Texas

MICRO-DESIGN
MDX-2
SYSTEM INTERFACE EXPANSION BOARD

prepared by:

MICRO-DESIGN
P.O. BOX 748
MANCHACA, TEXAS 78652
1 (512) 282-0225

Revision 1.5

Printed by C&J Enterprises P.O. Box 18982 Austin, TX 78760 (512) 445-6427

Table Of Contents

List Of Figures

1.0 INTRODUCTION

The MDX-2 is an expansion board designed to interface directly to your TRS-80 computer. It will enhance the capabilities of your basic system to that beyond any other expansion board available to date. We at MD feel it is by far the BEST buy on the market.

1.1 HARDWARE FEATURES

- o 32K Memory Expansion
- o On Board EPROM Capabilities
- o Direct Coupled Phone Modem (300 Baud)
- o Serial Port
- o Dual Cassette Line
- o Parallel Port
- o Real Time Clock
- o On Board Power Supply
- o Floppy Disk Controller

1.2 SOFTWARE FEATURES

- o Fully compatible with TRS-80 software

2.0 Design Overview

The MDX-2 is a bus extension to the TRS-80 computer. It was designed to be a low cost, modular system. Its modular design enables the user to assemble his board in the sequence he desires, at the time he desires. The basic modules are:

- o Power Supply
- o Phone Modem
- o Memory Expansion
- o EPROM
- o Real Time Clock
- o Serial Interface
- o Parallel Interface
- o Dual Cassette Line
- o Floppy Disk Controller

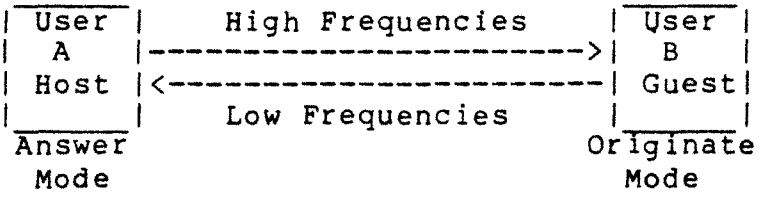
2.1 Power Supply

The power supply uses a TRS-80 Computer Transformer (cat #4000007) to supply raw DC to the regulators. An option to the Radio Shack transformer is discussed in section 4.4. There are four regulated supplies; +5,-5,+12 & -12 volts.

2.2 Phone Modem

The phone modem is a 300 baud, direct connect modem. It uses a Frequency Shift Keying (FSK) modulation scheme. Two frequencies, 200 Hz apart, are used where a logic 1 (MARK) is the higher frequency and a logic 0 (SPACE) is the lower frequency. Two pairs of frequencies are used for simultaneous two-way communications,which is called "Full Duplex" operation. The lower pair is used for transmitting and the higher pair for receiving. A modem operating in this mode is called an "Originate Mode" device, since the terminal is usually used to originate the call to the computer. This mode may be used if the user is talking to a "host" computer set up to talk to a standard 300 baud terminal. It is also used by one of the two users (A and B) as per the example

below (Fig 1). "Answer Mode" devices are just the opposite in that they transmit on the higher pair of frequencies and receive on the lower pair.



Dual Users Configuration

Fig. 1

Two TRS-80 users may communicate through the phone modem by designating one as the "host" (operates in the "answer mode"), and the other as the "guest" (operates in the "originate mode").

The phone modem may be used with the on-board serial circuit, or it may be connected to any RS232 port. Jumpers are provided for this option.

Since the phone modem is direct coupled to the phone line (i.e. no acoustic coupler is used), little or no noise will occur from outside interference. This results in very "quiet" modem operation.

This modem may also be used to communicate with both the Source and Compu-Serve* as well as any other 300 baud machine.

2.3 Memory Expansion

Memory can be expanded to 48K with the MDX-2. The first 16K must be added to the TRS-80. The second 16K is located at U30-U37 and the third 16K is at U20-U27 on the expansion board. Fig. 2 shows the memory map.

* Source and Compu-Serve are trademarks of their respective companies.

2.4 EPROM

A 2716 2K or 2532 4K EPROM option is offered for storage of user firmware. The EPROM sits in the upper most 2K of the memory map and is jumper selected. Single supply EPROM's are used. Modification for the new 4K EPROMS (MCM2532) is jumper selectable (see section 6.3.1).

2.5 Real Time Clock

Programming the Real-Time clock can be done in a user program or by using G2's Level III Basic *. The G2 program is much like Disk Basic and easy to use. A driver program may also be found in the Radio Shack Expansion Interface Board manual on pages 20-23.

The clock can be programmed to tell day, month and year, and can be used as a clock or a timer in any number of ways... controlling household appliances, turning on and off computer peripherals,....

2.6 Serial Interface

Serial interfacing is accomplished using a Western Digital TR1602B UART, a status buffer and a latch. The port can be configured for Data Terminal equipment (DTE) or Data Communications equipment (DCE) and is also baud rate selectable from 300 baud to 9600 baud. Parity, word length and stop bits are also hardware programmable.

2.7 Parallel Interface

This port provides parallel data that is compatible with Radio Shack line printers or any other printer that is Radio Shack compatible. The interface consist of an 8 bit output port and a four bit input port and is accessed through memory address 37E8 HEX.

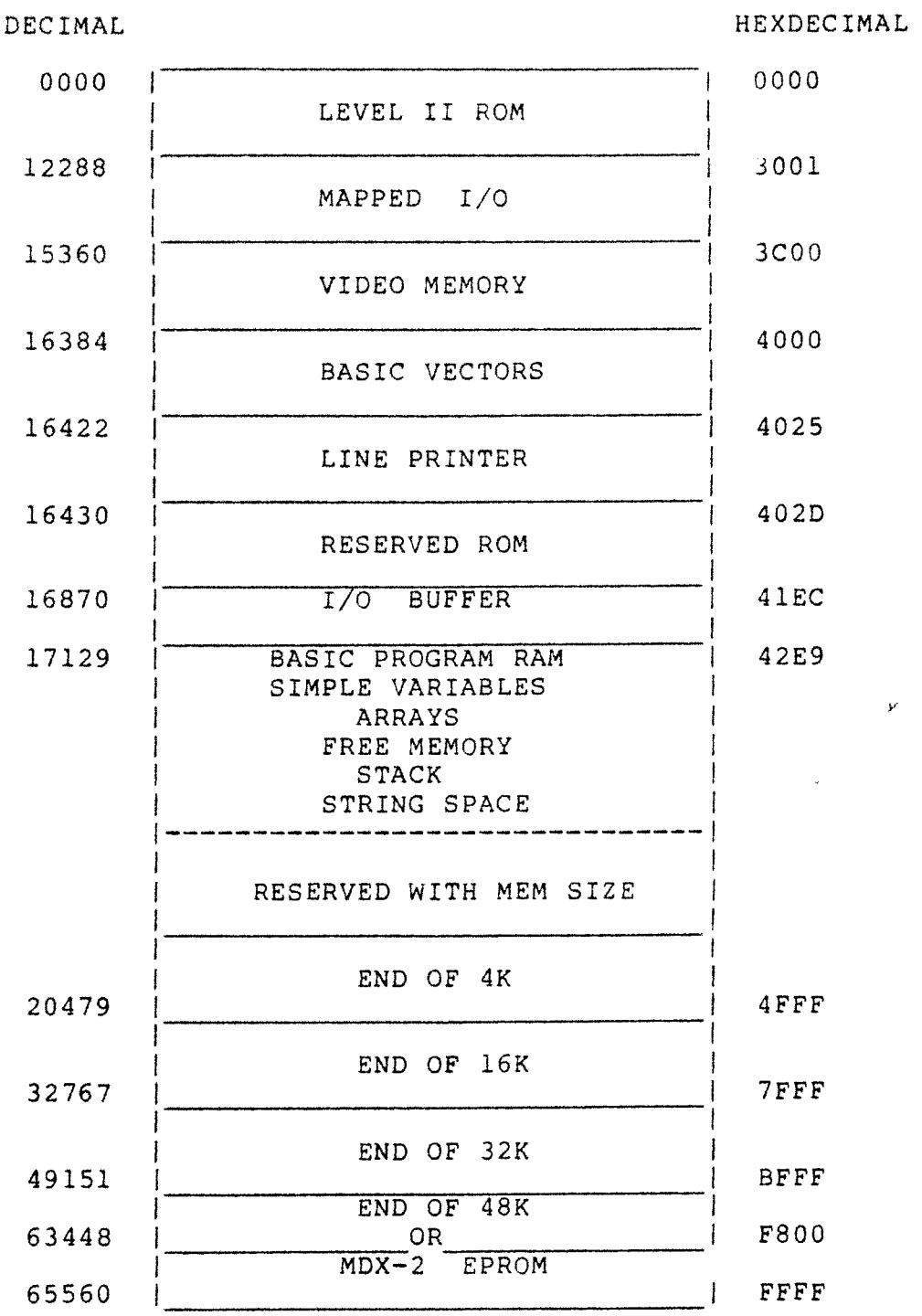
2.8 Dual Cassette Line

The Dual Cassette Option allows the user to software select between 2 cassette recorders. It can be done in either Basic or in assembly language. Some external logic is required (see Fig. 10).

2.9 Floppy Disk Controller

The heart of the MDX-2 Floppy Disk Controller is the Western Digital FD1771B. This 40 pin I.C. takes care of most of the functions of FDC, including cyclic redundancy checks, internal data/clock separation and all required logging of track location, sector location and I.D. field locations. Up to four floppy disk drives may be driven by the MDX-2. All TRS-80 compatible drives and all DOS software compatible with these drives will run with the MDX-2.

* G2 Level III Basic is a product of Micro-Soft



MDX-2 Memory Map

Fig. 2

3.0 Parts List

The following pages contain the parts lists. They are divided into three sections for the ease of finding parts. The three lists are:

1). Composite List
2). List By Sections
3). List By Numbers

The composite list is sorted by quantities of each part. This list is good for the user who plans to build the entire board. When all parts in the list are collected, the user is ready to assemble his board.

The list by sections should be used if the user plans to omit certain sections. This list gives the parts by sections. There are duplicates in this list where parts are used for more than one section.

The list by numbers should be used as a reference during trouble-shooting and when checking the locations of parts. It is sorted by device numbers.

There should be no substitutions to the parts list. 74ls parts must be used where called for. All 1% resistors MUST be the exact value called for . If parts called for in the parts list are used exclusively, trouble-free operation will result.

Parts List By Numbers

R1*	100	OHM	1/4 W	10%
R2*	100	OHM	1/4 W	10%
R3*	100	OHM	1/4 W	10%
R4*	100	OHM	1/4 W	10%
R5*	100	OHM	1/4 W	10%
R6*	100	OHM	1/4 W	10%
R7*	100	OHM	1/4 W	10%
R8*	100	OHM	1/4 W	10%
R9	220	OHM	1/4 W	10%
R10	220	OHM	1/4 W	10%
R11	220	OHM	1/4 W	10%
R12	680	OHM	1/4 W	10%
R13	680	OHM	1/4 W	10%
R14	150	OHM	1/4 W	10%
R15	1K	OHM	1/4 W	10%
R16	220	OHM	1/4 W	10%
R17	47	OHM	1/4 W	10%
R18	3K	OHM	1/4 W	10%
R19	220	OHM	1/4 W	10%
R20	15M	OHM	1/4 W	10%
R21	100K	OHM	1/4 W	10%
R22	560	OHM	1/4 W	10%
R23	22K	OHM	1/4 W	10%
R24	22K	OHM	1/4 W	10%
R25	2K	OHM	1/4 W	10%
R26	1K	OHM	1/4 W	10%
R27	680	OHM	1/4 W	10%
R28	1K	OHM	1/4 W	10%
R29	267	OHM	1/4 W	1%
R30	165K	OHM	1/4 W	1%
R31	18.7	OHM	1/4 W	1%
R32	324	OHM	1/4 W	1%
R33	210K	OHM	1/4 W	1%
R34	8.66K	OHM	1/4 W	1%
R35	619	OHM	1/4 W	1%
R36	95.3K	OHM	1/4 W	1%
R37	845	OHM	1/4 W	1%
R38	165K	OHM	1/4 W	1%
R39	21.5K	OHM	1/4 W	1%
R40	1.24K	OHM	1/4 W	1%
R41	237K	OHM	1/4 W	1%
R42	8.87K	OHM	1/4 W	1%
R43	2.55K	OHM	1/4 W	1%
R44	97.6K	OHM	1/4 W	1%
R45	10	OHM	2 W	10%
R46	10	OHM	2 W	10%
R47	1K	OHM	1/4 W	10%
R48	1K	OHM	1/4 W	10%
R49	1K	OHM	1/4 W	10%
R50	1K	OHM	1/4 W	10%
R51	1K	OHM	1/4 W	10%
R52	220	OHM	1/2 W	10%
R53	100K	OHM	1/4 W	10%
R54	1K	OHM	1/4 W	10%
R55	15K	OHM	1/4 W	10%
R56	20K	OHM	1/4 W	10%
R57	220	OHM	1/4 W	10%

* HEADER (R1-R8)

C1	27 PFD	
C2	0.1 UFD	
C3	0.1 UFD	
C4	1.0 UFD	
C5	.01 UFD	1%
C6	.01 UFD	1%
C7	1.0 UFD	ELECTROLYTIC @ 16
C8	.01 UFD	1%
C9	.01 UFD	1%
C10	.01 UFD	1%
C11	.01 UFD	1%
C12	.01 UFD	1%
C13	.01 UFD	1%
C14	1.0 UFD	ELECTROLYTIC @ 16
C15	.01 UFD	1%
C16	.01 UFD	1%
C17	.01 UFD	1%
C18	.01 UFD	1%
C19	220 UFD	ELECTROLYTIC @ 16
C20	220 UFD	ELECTROLYTIC @ 16
C21	50 UFD	ELECTROLYTIC @ 25
C22	50 UFD	ELECTROLYTIC @ 25
C23	3300 UFD	ELECTROLYTIC @ 35
C24	6.8 UFD	TANTALUM @ 16V
C25	6.8 UFD	TANTALUM @ 16V
C26	6.8 UFD	TANTALUM @ 16V
C27	6.8 UFD	TANTALUM @ 16V
C28	6.8 UFD	TANTALUM @ 16V
C29	6.8 UFD	TANTALUM @ 16V
C30	6.8 UFD	TANTALUM @ 16V
C31	6.8 UFD	TANTALUM @ 16V
C32	1.0 UFD	ELECTROLYTIC @ 16
C33	6.8 UFD	TANTALUM @ 16V
C34	6.8 UFD	TANTALUM @ 16V
C35	6.8 UFD	TANTALUM @ 16V
C36	6.8 UFD	TANTALUM @ 16V
C37	6.8 UFD	TANTALUM @ 16V
C38	6.8 UFD	TANTALUM @ 16V
C39	6.8 UFD	TANTALUM @ 16V
C40	6.8 UFD	TANTALUM @ 16V
C41	0.1 UFD	
C42	0.1 UFD	
C43	0.1 UFD	
C44	0.1 UFD	
C45	0.1 UFD	
C46	0.1 UFD	
C47	0.1 UFD	
C48	0.1 UFD	
C49	0.1 UFD	
C50	220 UFD	
C51	0.1 UFD	
C52	NOT USED	
C53	NOT USED	
C54	220 PFD	CERAMIC DISK
C55	3300 UFD	ELECTROLYTIC @ 35
C56	0.1 UFD	
C57	0.1 UFD	

Parts List By Numbers
(continued)

R58	1K OHM	1/4 W	10%	
R59	1K OHM	1/4 W	10%	
R60	1K OHM	1/4 W	10%	
R61	1K OHM	1/4 W	10%	
R62	1K OHM	1/4 W	10%	
R63	1K OHM	1/4 W	10%	
R64	10 OHM	1/4 W	10%	
R65	1K OHM	1/4 W	10%	
R66	10K OHM	1/4 W	10%	
R67	10 OHM	1/4 W	10%	
R68	1K OHM	1/4 W	10%	
R69	10K OHM	1/4 W	10%	
R70	150 OHM	1/4 W	10%	
R71	150 OHM	1/4 W	10%	
R72	150 OHM	1/4 W	10%	
R73	150 OHM	1/4 W	10%	
R74	10K OHM	1/4 W	10%	
R75	10K OHM	1/4 W	10%	
R76	NOT USED			
R77	200K OHM	1/4 W	10%	
R78	1K OHM	1/4 W	10%	

C58	0.1 UFD	
C59	0.1 UFD	
C60	0.1 UFD	
C61	0.1 UFD	
C62	0.1 UFD	
C63	0.1 UFD	
C64	0.1 UFD	
C65	0.1 UFD	
C66	0.1 UFD	
C67	0.1 UFD	
C68	0.1 UFD	
C69	0.1 UFD	
C70	0.1 UFD	
C71	0.1 UFD	
C72	0.1 UFD	
C73	0.1 UFD	
C74	0.1 UFD	
C75	0.1 UFD	
C76	0.1 UFD	
C77	0.1 UFD	
C78	0.1 UFD	
C79	0.1 UFD	
C80	0.1 UFD	
C81	0.1 UFD	
C82	0.1 UFD	
C83	0.1 UFD	
C84	0.1 UFD	
C85	0.1 UFD	
C86	0.1 UFD	
C87	0.1 UFD	
C88	0.1 UFD	
C89	0.1 UFD	
C90	0.1 UFD	
C91	0.1 UFD	
C92	0.1 UFD	
C93	0.1 UFD	
C94	0.1 UFD	
C95	0.1 UFD	
C96	1.0 UFD	ELECTROLYTI @ 16V
C97	0.1 UFD	
C98	33 UFD	ELECTROLYTI @ 6V
C99	0.1 UFD	
C100	0.1 UFD	
C101	0.1 UFD	
C102	0.1 UFD	
C103	0.1 UFD	
C104	0.1 UFD	
C105	0.1 UFD	
C106	0.1 UFD	
C107	0.1 UFD	

NOTES UNLESS OTHERWISE STATED :

ALL RESISTORS ARE 1/4 W , 10 % , CARBON
ALL CAPACITORS ARE UPD , 20 % , 25 V

Parts List By Numbers
(continued)

___	U1	74LS241
___	U2	74LS241
___	U3	74LS245
___	U4	74LS175
___	U5	74LS175
___	U6	74LS367
___	U7	74LS123
___	U8	74LS139
___	U9	74LS30
___	U10	74LS32
___	U11	74LS02
___	U12	74LS244
___	U13	1K RESISTOR PACK (See Fig. 4)
___	U14	74S04
___	U15	74LS161
___	U16	74LS161
___	U17	7493A
___	U18	7493A
___	U19	74LS08
___	U20	MC4116
___	U21	MC4116
___	U22	MC4116
___	U23	MC4116
___	U24	MC4116
___	U25	MC4116
___	U26	MC4116
___	U27	MC4116
___	U28	DIP SWITCH
___	U29	DIP SWITCH
___	U30	MC4116
___	U31	MC4116
___	U32	MC4116
___	U33	MC4116
___	U34	MC4116
___	U35	MC4116
___	U36	MC4116
___	U37	MC4116
___	U38	7490
___	U39	7492
___	U40	74LS74
___	U41	74LS155
___	U42	74LS74
___	U43	74LS04
___	U44	74LS30
___	U45	74LS244
___	U46	MC1489
___	U47	74LS367
___	U48	74LS367
___	U49	74LS175
___	U50	MC1488
___	U51	MC1489
___	U52	74LS155
___	U53	TR1602B (WESTERN DIGITAL)
___	U54	75452
___	U55	74LS367
___	U56	MC1458
___	U57	MC14412
___	U58	MC1458
___	U59	MC1458
___	U60	MC1458
___	U61	MLM311P1
___	U62	7812 +12 VOLT REGULATOR
___	U63	7912 -12 VOLT REGULATOR
___	U64	DIP SWITCH
___	U65	Ua78H05 5V-5A REGULATOR (FAIRCHILD) or EQUIV. (LM723K) (3 AMP MIN.)
___	U66	74LS30
___	U67	2716 EPROM OR MCM2532 (4K)
___	U68	74LS04
___	U69	7438
___	U70	74LS04
___	U71	FD1771-01B or EQUIV.
___	U72	7438
___	U73	7438
___	U74	74LS04
___	U75	74LS175
___	U76	74LS240
___	U77	74LS240
___	U78	74LS04 OR 74LS14
___	U79	74S32
___	U80	74LS08
___	Y1	4 MHZ XTAL
___	Y2	1 MHZ XTAL
___	CR1	DIODE BRIDGE (RS #276-1146)
___	D1	1N4733B (5.1V ZENER)
___	D2	1N4001
___	D3	1N4001
___	T1	TRS-80 COMPUTER TRANSFORMER RS #4000007
___	F1	2A FUSE
___	SW1	3P2T SWITCH (C&K #7301)
___	6	8 PIN SOLDER-TAIL SOCKETS
___	26	14 PIN SOLDER-TAIL SOCKETS
___	36	16 PIN SOLDER-TAIL SOCKETS
___	7	20 PIN SOLDER-TAIL SOCKETS
___	1	24 PIN SOLDER-TAIL SOCKETS
___	2	40 PIN SOLDER-TAIL SOCKETS
___	2	TO-220 HEAT SINKS
___	1	TO-3 HEAT SINK
___		RS-232 CONECTOR MALE AMP #206604-1 FEMALE AMP #206584-1
___	2	FUSE HOLDER CLIPS
___	1	16 PIN HEADER PLATFORM

Parts List By Sections

The user should be careful when using this list. Remember to consider all sections you will need. For example, if you plan on using the phone modem with the on-board serial port, you must aquire parts for both sections, but not the duplicate parts (i.e. C69, U50...). The power supply is required for all sections.

After deciding on the sections you will build, use this list to update the List By Numbers, i.e. mark with an x the parts you will need on the List By Numbers. Then use that list to accumilate your parts, putting a check mark by each part as it is aquired. This process will help to avoid buying duplicate parts.

POWER SUPPLY

___ C19-C23	___ R45	___ U62	___ D1
___ C49-C51	___ R46	___ U63	___ D2
___ C55	___ R52	___ U65	___ D3
___ C95		___ CR1	___ T1 (TRANSFORMER)
			___ F1 (AND HOLDER)

MEMORY

___ C24-C31	___ C66	___ R1-R11	___ U1-U3
___ C33-C48	___ C68	___ R57	___ U8-U12
___ C52	___ C69	___ R59-R63	___ U19-U27
___ C53	___ C71-C73	___ R64	___ U30-U37
___ C56	___ C92	___ R67	___ U43
___ C65			

EPROM

___ C56	___ U12	___ U66
___ C70	___ U14	___ U67

MODEM

- ___ C2-C18
- ___ C32
- ___ C63
- ___ C96
- ___ R20-R44
- ___ R53-R55
- ___ U50
- ___ U51
- ___ U56-U61
- ___ Y2
- ___ SW1

SERIAL PORT

- ___ C1
- ___ C53
- ___ C57
- ___ C59
- ___ C60-C62
- ___ C67
- ___ C69
- ___ C74-C78
- ___ C92
- ___ R12-R14
- ___ R16-R19
- ___ R47-R51
- ___ R68
- ___ R66
- ___ U14-U19
- ___ U28-U29
- ___ U43-U54
- ___ U64
- ___ U68
- ___ U70
- ___ Y1

LINE PRINTER BUS

- ___ C54
- ___ C56
- ___ C71-C72
- ___ C79-C82
- ___ C86
- ___ C87
- ___ R1-R11
- ___ R56-R62
- ___ U4-U9
- ___ U12-U14
- ___ U41

REAL TIME CLOCK

- ___ C1
- ___ C64
- ___ C81
- ___ C83-C85
- ___ C88-C94
- ___ R12-R15
- ___ R65
- ___ R66
- ___ Y1
- ___ U13
- ___ U15-U19
- ___ U38-U42
- ___ U55
- ___ U69
- ___ U78-U79

CASSETTE OPTION

- ___ C72
- ___ C71
- ___ C56
- ___ C56
- ___ C82
- ___ C81
- ___ U8
- ___ U9
- ___ U12
- ___ U14
- ___ U41

FLOPPY-DISK

- ___ MEMORY SECTION
- ___ REAL TIME CLOCK
- ___ C97-C107
- ___ R69-R78
- ___ U71
- ___ U72
- ___ U73
- ___ U74
- ___ U75
- ___ U76
- ___ U77
- ___ U78
- ___ U79
- ___ U80

Composite Parts List

DISCRIPTION	QUANTITY	SYMBOLICS
100 OHM 1/4 WATT 10%	8	R1-R8
220 OHM 1/4 WATT 10%	6	R9-R11,R16,R19,R57
680 OHM 1/4 WATT 10%	3	R12,R13,R27
150 OHM 1/4 WATT 10%	5	R14,R70-73
10K OHM 1/4 WATT 10%	1	R66,R74,R75
3K OHM 1/4 WATT 10%	1	R18
15M OHM 1/4 WATT 10%	1	R20
100K OHM 1/4 WATT 10%	2	R21,R53
200K OHM 1/4 WATT 10%	1	R77
560 OHM 1/4 WATT 10%	1	R22
22K OHM 1/4 WATT 10%	2	R23,R24
2K OHM 1/4 WATT 10%	1	R25
20K OHM 1/4 WATT 10%	1	R56
15K OHM 1/4 WATT 10%	1	R55
267 OHM 1/4 WATT 1%	1	R29
165K OHM 1/4 WATT 1%	2	R30,R38
18.7 OHM 1/4 WATT 1%	1	R31
324 OHM 1/4 WATT 1%	1	R32
210K OHM 1/4 WATT 1%	1	R33
8.66K OHM 1/4 WATT 1%	1	R34
619 OHM 1/4 WATT 1%	1	R35
95.3K OHM 1/4 WATT 1%	1	R36
845 OHM 1/4 WATT 1%	1	R37
21.5K OHM 1/4 WATT 1%	1	R39
1.24K OHM 1/4 WATT 1%	1	R40
237K OHM 1/4 WATT 1%	1	R41
8.87K OHM 1/4 WATT 1%	1	R42
2.55K OHM 1/4 WATT 1%	1	R43
97.6K OHM 1/4 WATT 1%	1	R44
10 OHM 2 WATT 10%	2	R45,R46
220 OHM 1/2 WATT 10%	1	R52
47 OHM 1/4 WATT 10%	1	R17
10 OHM 1/4 WATT 10%	2	R64,R67
1K OHM 1/4 WATT 10%	19	R15,R26,R28,R47-R51, R54,R58-R63,R65,R68, R78
.01 UFD 1%	12	C5,C6,C8-C13,C15-C18
1.0 UFD ELECTROLYTIC @ 16V	4	C4,C7,C14,C32,C96
27 PFD	1	C1
220 UFD ELECTROLYTIC @ 16V	3	C19,C20,C50
50 UFD ELECTROLYTIC @ 25V	2	C21,C22
3300 UFD ELECTROLYTIC @ 35V	2	C23,C55
6.8 UFD TANTALUM @ 16V	16	C24-C31,C33-C40
0.1 UFD	60	C2,C3,C41-C48,C51, C56-C95,C97,C99-C107
220 PFD CERAMIC DISK	1	C54
33 UFD ELECTROLYTIC @ 6V	1	C98

Composite Parts List
(continued)

	DISCRIPTION	QUANTITY	SYMBOLICS
____	74s04	1	U14
____	74LS02	1	U11
____	74LS04	5	U43,U68,U70,U74,U78
____	74LS08	2	U19,U80
____	74LS30	3	U9,U44,U66
____	74S32	1	U79
____	74LS32	1	U10
____	74LS74	2	U40,U42
____	74LS123	1	U7
____	74LS139	1	U8
____	74LS155	2	U41,U52
____	74LS161	2	U15,U16
____	74LS175	4	U4,U5,U49,U75
____	74LS240	2	U76,U77
____	74LS241	2	U1,U2
____	74LS244	2	U12,U45
____	74LS245	1	U3
____	74LS367	4	U6,U47,U48,U55
____	7438	3	U69,U72,73
____	7490	1	U38
____	7492	1	U39
____	7493A	2	U17,U18
____	75452	1	U54
____	FD1771-01B	1	U71
____	MC4116,2117 OR EQUIV.	16	U20-U27,U30-U37
____	MC1458	4	U56,U58-U60
____	MC1488	1	U50
____	MC1489	2	U46,U51
____	MC14412	1	U57
____	TR1602B WESTERN DIGITAL	1	U53
____	MLM311P1	1	U61
____	2716 EPROM	1	U67
____	7812 12V REGULATOR	1	U62
____	7912 -12V REGULATOR	1	U63
____	Ua78H05 5V 5A REGULATOR	1	U65
____	DIP SWITCH SPST	3	U28,U29,U64
____	1K RESISTOR PACK (16 PIN)	1	U13
____	4 MHZ CRYSTAL	1	Y1
____	1 MHZ CRYSTAL	1	Y2
____	DIODE BRIDGE (RS#276-1146)	1	CR1
____	1N4001	2	D2,D3
____	1N5231B (5V ZENER)	1	D1
____	3P2T SWITCH	1	SW1
____	2A FUSE	1	F1
____	TO-220 HEAT SINKS	2	
____	TO-3 HEAT SINK	1	
____	RS-232 CONECTOR	1	
____	FUSE HOLDER CLIPS	2	
____	8 PIN SOLDER-TAIL SOCKETS	6	
____	14 PIN SOLDER-TAIL SOCKETS	26	
____	16 PIN SOLDER-TAIL SOCKETS	36	
____	20 PIN SOLDER-TAIL SOCKETS	7	
____	24 PIN SOLDER-TAIL SOCKETS	1	
____	40 PIN SOLDER-TAIL SOCKETS	2	

4.0 Assembly

4.1 Overveiw

As stated before, the MDX-2 may be assembled in sections at the users discretion. There are certain parts that are required for all sections i.e. the power supply (see "Parts List By Sections" for exact parts required).

The user should decide which sections he desires to build and accumulate ALL parts required for that section before starting assembly. You should use the "Composite Parts List" to acquire your parts, and use the "List By Numbers" to populate your board. Check off each component as you install it. This is to insure no component is left off during assembly.

Before assembly begins, take a few minutes to visually inspect the expansion board. This will keep debug time down to a minimum. We feel that if you follow the instructions closely, you will have no problems.

It is assumed that the user has a certain degree of knowledge of the tools necessary to build the board; i.e. soldering iron and soldering techniques. Be very careful not to damage the traces or pads. They are VERY delicate. Excessive heat is unnecessary, and WILL damage them. Use a 40-50 watt iron for construction. DO NOT USE A SOLDER-GUN!!

It is imperative that sockets be installed for all I.C.'s. This will simplify troubleshooting and repair later.

The step-by-step assembly instructions follow. Check off each step as it is completed. This will help you complete the assembly faster and more efficiently.

4.2 Assembly Instructions

____ Inspect your board for bad plate-thru's, bad solder-mask area's and general appearance.

____ Sort your parts into resistors, capacitors, sockets, ect.

____ Install all applicable I.C. sockets: starting in the upper left-hand corner, insert the appropriate size socket in the board and bend over the corner leads of the socket. This will hold it in place when you turn over the board. Repeat this proceedure for all sockets.

____ Turn the board over and solder all sockets in the board. Be careful not to cause solder bridges. Do not leave the soldering iron on too long as this may cause solder to flow thru the holes to the top side of the board and cause a short under the socket. Snip the leads off as close to the board as possible.

____ Inspect board for cold solder joints and solder bridges.

____ Install all applicable resistors (see parts list). Starting with R1, check resistor for correct value, bend the leads with a pair of long-nose pliers to fit the appropriate holes, and insert the resistor in its place. Then bend the leads over so the part will stay in the board. Now mark off R1 in the "Parts List By Numbers". Repeat this proceedure for 5 to 10 resistors. Recheck the resistors for correct value.

____ Turn the board over and solder these resistors in. Snip off the leads as close to the pads as possible. Repeat these last two steps until all resistors are installed.

____ Install all applicable capacitors (see parts list). Starting with C1, check the capacitor for correct value, bend the leads with a pair of long-nose pliers to fit the appropriate holes, and insert the capacitor in its place (WATCH POLARITIES were applicable). Then bend the leads over so the part will stay in the board. Now mark off C1 in the "Parts List By Numbers". Repeat this proceedure for 5 to 10 capacitors. Recheck the capacitors for correct value.

____ Turn the board over and solder these capacitors in. Snip off the leads as close to the pads as possible. Repeat these last two steps until all capacitors are installed.

____ Install voltage regulators U62 and U63. The silk-screen on the board shows the correct placement of these parts. Place the board in front of you on the table with "MDX2" in the lower right- hand corner. Now install U62 and U63 so that the metal tab is to the right. Solder these two in the board. Snip off the leads as close as possible to the board.

____ Install regulator U65 and heat sink. THE HEAT SINK IS ABSOLUTELY REQUIRED. Using heat sink compound, install the regulator and heat sink on the board and secure with two #4 nuts and bolts. Solder the leads on the back and snip off excess leads.

____ Install crystals Y1 and Y2. Solder the leads on the back of the board. Snip off excess leads.

____ Install diodes D1, D2 and D3. NOTE POLARITIES. The little white band on one end of the diodes distinguishes the polarity. The lead closest to this ring should be inserted in the hole indicated by the white stripe on the silk-screen. Insert D1 in its place and bend the leads to hold it in the board. Then invert the board, solder the leads and snip off the excess leads. Repeat for D2 and D3.

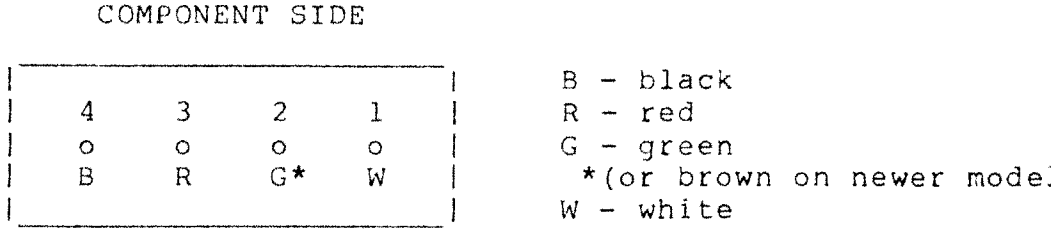
____ Install bridge rectifier on the board. NOTE POLARITY. The positive (+) lead of the rectifier goes in the hole mark with "+". Solder and snip excess leads off.

____ Install fuse clips in the board and solder in place.

____ It is advised that you put some sort of stand-offs on your board to reduce the possibility of a short on the bottom of the board. Five mounting holes are provided for this. They are in the four corners of the board and one in the middle of the board.

____ DO NOT INSTALL ANY JUMPERS OR I.C.'s AT THIS TIME!!!

The transformer, as supplied by Radio Shack, normally connects through a DIN plug. To connect power to the board, it is necessary to remove this DIN plug from the transformer cord. When this is accomplished, connect the four wires as shown in Fig. 3. [If a Radio Shack Computer Transformer is not available, a 25.2V 2 amp center-tapped transformer and 2 1N4007 diodes may be substituted. See section 4.4 for details.]

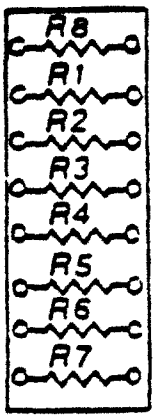


Power Connection To J-1

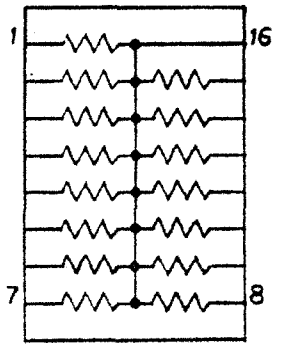
Fig. 3

4.3 Header Construction

A 16 pin header is used to hold R1-R8. It should be constructed at this point. See Fig. 4 for construction details. Do not install this header until I.C. installation is called for.



Header Construction

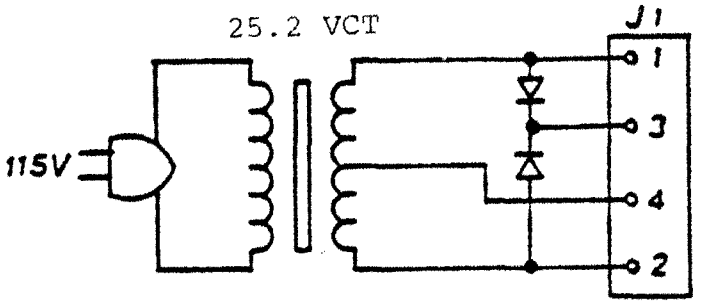


U13 Resistor Pack Configuration

Fig. 4

4.4 Transformer (Optional)

An option to using the TRS-80 Computer Transformer is to build up the following circuit. By using an 25.2VCT (center-tapped) 2 amp transformer, (RS #273-1512), two diodes (1N4007) and a power cord, you can achieve a better source of power for your MDX board. Build the circuit described in Fig. 5. Be extra careful to get the diodes polarity correct!



Transformer Construction

Fig. 5

5.0 System Initialization

The following section assumes that the user has installed all sockets, resistors, capacitors, and all hardware required for the options selected and the required sections. (NO I.C.'s).

If the sequence described below is followed, system initialization will be quick and easy.

5.1 Power Supply

1). Check J-1 for proper hook-up (See Fig. 3)

2). DO NOT INSTALL ANY JUMPERS

3). Using a voltmeter, check voltages at the following locations by first putting the leads on the appropriate jumper pad, and then applying the power. If the correct voltage is not present, TURN OFF POWER IMMEDIATELY and check component placements and values.

A). +5 volts between jumper 7 and the negative side of C23

B). -5 volts between jumper 5 and the negative side of C23

C). +12 volts between jumper 3 and the negative side of C23

D). -12 volts between jumper 1 and the negative side of C23

When these readings are verified, install jumpers wires (JUMPERS ARE INDICATED BY CIRCLES ON THE P.C. BOARD):

1). jumper 1 to jumper 2

2). jumper 3 to jumper 4

3). jumper 5 to jumper 6

4). jumper 7 to jumper 8

After these jumpers have been installed, you are ready to proceed. Apply power and recheck step 3 for proper voltages. If you do not have all of them TURN OFF POWER. Check the resistors and capacitors for proper values and be sure they are installed correctly (WATCH POLARITIES!).

If all voltages are present, install all applicable I.C.'s (watch for bent pins and correct orientation; i.e. pin 1 in correct position). Now apply power and check for the four voltages again (step 3). If they are not present POWER DOWN. Check for I.C.'s installed backwards.

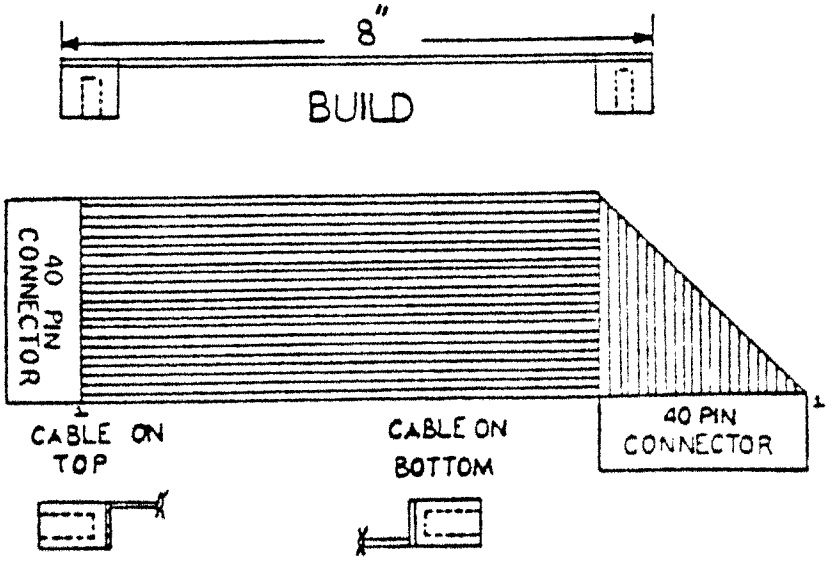
When all voltages are present, power down and proceed to next section.

5.2 Cable Construction

A cable is required for the connection to the TRS-80 computer. This may be purchased from your local computer shop, or you may want to build your own. If you decide to build it, use flat ribbon cable and make it no longer than 8". Check the continuity between each corresponding pin before using your cable (see Fig. 6). The length of this cable may be critical, especially on older model TRS-80's. Make it as short as possible.

5.3 Connection To The TRS-80

When connecting the cable to the computer, care must be taken to insure that pin one of the TRS-80 keyboard is connected to pin one of the MDX-2. With the component side up, there should be a twist in the cable (see Fig. 6).



Cable Connection To The TRS-80

Fig. 6

5.4 System Power-Up

It is required that your system be powered up in a certain sequence to ensure proper operation. This is due to the way the TRS-80 comes out of reset. First turn on the monitor, then the MDX-2 and then the TRS-80 keyboard. With the MDX-2, holding in the break key is required if the FDC circuit is not built up.

The screen should display:

```
MEM SIZE?
MEM SIZE?_
```

Now press the <enter> key and in a few seconds your prompt should be:

```
READY _
```

Now type:

```
?MEM <enter>
```

The display should show greater than 48000 in a 48K system
The display should show greater than 31000 in a 32K system
The display should show greater than 15000 in a 16K system

(These figures will change if the EPROM is enabled).

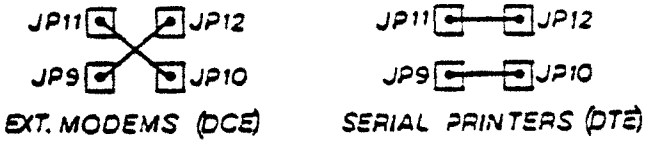
This number shows the available users memory. Anything less than these figures indicate memory and/or address decode problems. Running a memory test program is highly recommended to insure all memory chips are good. You may have to add C52 and C53 (2-2200 PFD caps) to make your memory operational. This is only necessary on a few models. If your memory does not come up and you feel you have this problem, please call us for further details.

The following sections assume that the interface has passed the memory size question.

5.5 Serial Port Test

The serial port is tested by looping the output data from the UART back to the input pin. Put a jumper wire from jumper 11 to jumper 9 (see Fig. 7). The baud rate switches should be set to transmit and receive at the same rate.

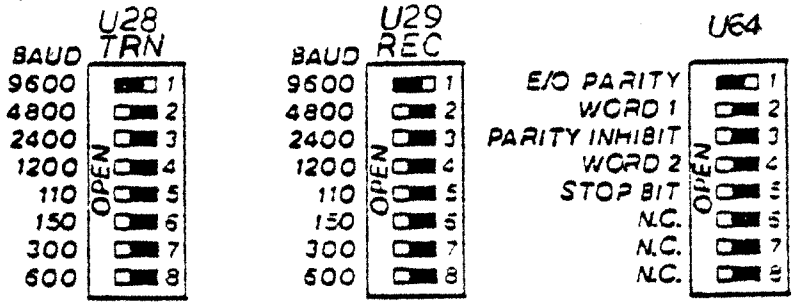
NOTE: Never select more than one baud rate per set of switches (one receive and one transmit) as this may damage devices on the board. The example in Fig. 8 is set up for 9600 baud transmit and 9600 baud receive.



Serial Port Jumpers Configuration

Fig. 7

After you have set your switches, you must load a serial driver program. The program in the appendix may be used or there are many available on the market that can be used. After the program has been loaded and is initialized, anything typed on the keyboard should be displayed on the screen.



Baud Rate And Serial Options Switches

Fig. 8

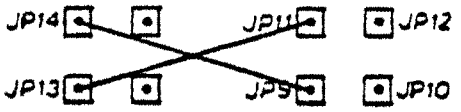
5.5.1 Phone Modem Test

The phone modem is tested using the Serial Port. For this reason, the Serial Port must have already been tested.

Jumper the modem to the Serial Port by connecting jumper 9 to jumper 14 and jumper 11 to jumper 13 (see Fig. 9). Then remove U57 (with power off) and bend up pins 2 and 10. Replace U57. Now tie pin 2 to 5 volts and pin 10 to ground. This will put the 14412 Modem chip in the test mode. Now power up the system and re-load the serial driver program. After initializing the program, any character typed will appear on the screen. After the phone modem has been deemed good, disconnect pins 2 and 10 of U57 and bend them back down. Replace U57.

Connection to the phone line requires a 600 OHM 1:1 transformer, a switch, and the appropriate phone jacks. See schematic for details.

If, during operation, noise is present (i.e. bad characters), R22 should be replaced with a 600 ohm resistor. This compensates for a noisy phone line.



Modem Jumpers Configuration

Fig. 9

5.6 Parallel Port Test

Connect the printer cable to connector P3. Be sure that pin 1 of the cable connects to pin 1 of P3. After connecting the cable, apply power in this order:

1). Turn on printer
2). Turn on the video monitor
3). Turn on floppy-disk
4). Turn on the MDX-2
5). Turn on the TRS-80

In basic, enter the following lines:

```
10 LPRINT " HELLO , I AM READY TO PRINT "
20 END
```

Now run the program. It should output to the printer:

```
HELLO , I AM READY TO PRINT
```

5.7 Cassette Option Test

To use this port, add the logic shown in Fig. 10. Be sure to use a relay that energizes at 5 volts.

To test the cassette option, connect two tape recorders as shown in Fig. 10. Place a programmed tape in cassette #1 and press the PLAY button. Then place a blank tape in cassette #2 and press the RECORD and PLAY buttons.

In Basic type:

```
CLOAD # - 1, "A"
```

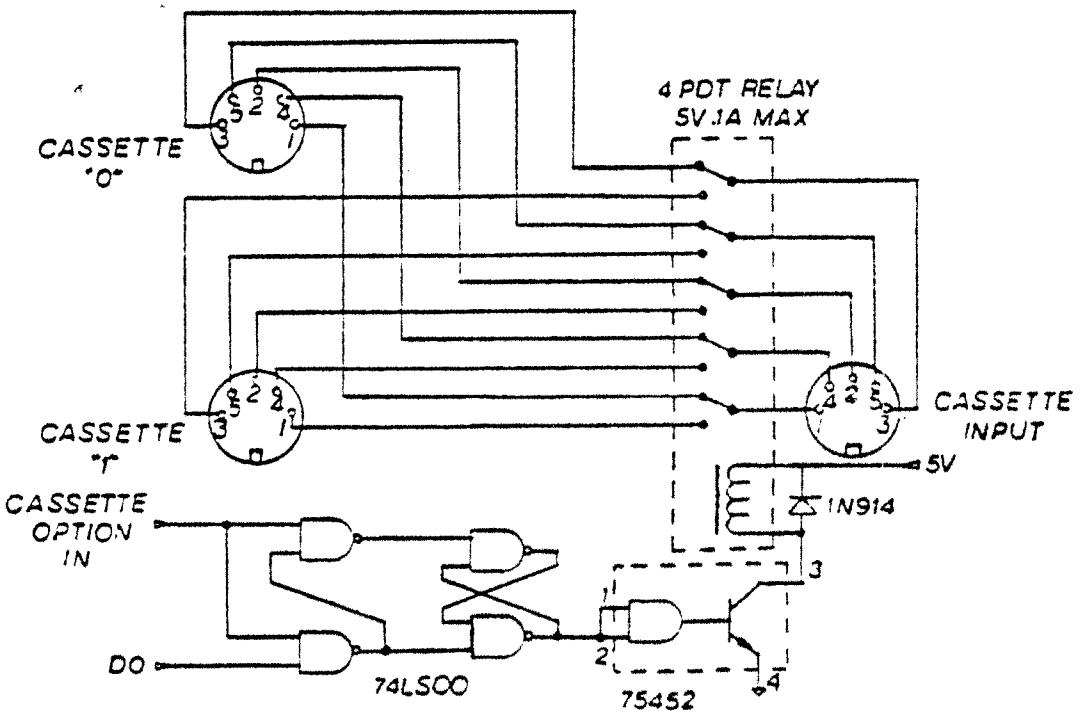
This loads the program on the tape into memory. Now type:

```
CSAVE # - 2, "A"
```

This records the program onto cassette #2. When it is complete, verify that the program is on cassette #2 by powering down (this erases memory) and reload the program from cassette #2.

```
CLOAD # - 2, "A"
```

The Dual Cassette option is very useful for backing up tapes, and since it is software programmable, you can use one for input data and the other for output data in the same program.



Dual Cassette - Users Logic

Fig. 10

5.8 EPROM Test

To test the EPROM option, simply install a programmed EPROM (2K or 4K). Connect jumper 15 to jumper 16. This enables the EPROM and disables memory in the space used by the EPROM. If a 4K EPROM is used, see section 6.3.1 to set up the jumpers.

Either a System command or a USR command may be used to test the contents of the EPROM.

When using the USR command, you must enter the origin (ORG) of your program MINUS ONE in the power-up question (MEM SIZE?). For example; If you originate a program at F800, then before you execute the program, you must have answered the "MEM SIZE?" with 63487.

```
63488  =  F800
-   1
-----
63487
```

This reserves memory from F800 to FFFF for the EPROM, otherwise the CPU will try to use this area for its Stack.

To use the USR command in Basic, you must first Poke the DECIMAL equivalent of the origination (org.) address into Basic.

```
POKE 16526, LSB          This is the org. of the program
POKE 16527, MSB          It must be above F7FF
```

Here is an example for a program originating at F800:

```
10  CLS
20  PRINT " THIS IS A TEST OF THE EPROM "
30  POKE 16526,00          REM 00
40  POKE 16527,248         REM F8
50  INPUT " PRESS [ENTER] TO GO TO PROGRAM IN EPROM ";A$
60  X = USR(1)
70  END
```

Now type RUN to execute the program.

To use the EPROM with a System command, simply enter the DECIMAL starting address:

```
READY _  [SYSTEM] [ENTER]

*? [/63488] [ENTER]    This is the decimal equivalent of F800
```

The program will begin execution.

5.9 Floppy Disk Controller Test

Connect a mini-floppy drive cable to connector P5 on your MDX-2, making sure that pin 1 of your floppy disk drive connects to pin 1 of P5. Insert a disk (write protected... i.e. write protection tab on). Now power up the TRS-80 . The drive should be selected and the motor activated. After a second, the DOS prompt should appear on the screen (this will vary between different DOS programs. See your DOS manual for details). To test the write capabilities, make a back-up copy of a DOS system diskette. Once again, see your DOS manual for further details.

6.0 Circuit Description

The following is a circuit description of the MDX-2. It is provided as an aid in trouble-shooting the board and enabling the user to better understand the product. The schematic should be used to follow the descriptions.

6.1 Memory Expansion Circuit

Memory starts at 8000 (hex) and goes to FFFF (see Fig 2). The address space is decoded by U8 and the resulting decode is present on U8-6 and U8-7, 32K and 48K enables respectfully. The output U8-7 must also be decoded for the EPROM option through U10, ANDed with the decode from U66 (see EPROM Circuit Description).

The addresses are buffered through U1 and U2 which are latched by the TRS-80 signal MUXB. Data is transferred through U3, a bi-directional buffer, and is enabled by a signal from U11-1. This signal is the 32K and 48K enables NORed with RDB (read). A high on U3-1 enables data to transfer from memory to the data bus and a low reverses the data flow from data bus to memory. RASB, CASB, WDB and MUXB are buffered through U12 and are terminated to reduce noise.

Series resistor R1-R7 are used as terminators to reduce signal ringing caused when interfacing TTL devices with MOS devices, resulting in a quieter memory array.

To provide for slower memories, the "Early Write" mode used. This means WB must lead CASB by 20ns. Another advantage of this mode is the ability to tie data-in and data-out together.

6.2 Parallel Line Printer Bus

The MDX-2 Line Printer Bus is designed for use with the Radio Shack parallel line printers. Other printers are easily adaptable to the interface. The interface consist of an 8 bit output port and a 4 bit printer status port.

The port is accessible through address 37E8 (hex). A write to this address is decoded through U41 and the resulting enable is on U41-11. This signal will load output latches U4 and U5, and causes U7 to produce a DATA STROBE and transfer the data to the printer. DATA STROBE is a low-going signal approximately 1.5 microseconds long.

A read of address 37E8 (hex) decodes through U41 (as did the write) to give the enable signal on U41-5. This signal enables U6 to latch 4 bits of data from the printer. These four bits make up the Printer Status Register (U6). They are described in Fig. 11.

DATA BIT	PRINTER STATUS
D7	Printer Busy
D6	Paper Empty
D5	Unit Select
D4	Fault

Parallel Port Status Bits

Fig. 11

The Radio Shack printer is internally wired such that the Printer Busy signal and the Paper Empty Signal are ORed together. Consequently the user need only read one of these (D7 or D6) before writing to the printer data latches. A logic 1 indicates Printer Busy. The Unit Select and Fault Status bits are not used on the Radio Shack printer.

The Radio Shack printer recognizes A0 (hex) as a line feed and a 0D (hex) as a carriage return. When the printer receives either of these, it it will set (logic 1) the Printer Busy Status bit, thus informing the users program it is busy.

6.3 EPROM Circuit Description

A 2716 (2K) or MCM2532 EPROM (4K) may be directly addressed by the user. U66 is used to decode addresses F800-FFFF. The output pin U66-8 has the dual purpose of enabling and disabling the memory space in the upper 2K of memory.

When jumper 15 to jumper 16 is open (no jumper wire connected), the EPROM is disabled by the pull-up resistor R52 which puts a logic 1 on the low enabled G (gate). This logic 1 also causes the RAM to be selected for this address space. When the jumper is inserted, the opposite effect occurs, i.e. the EPROM is now selected in this address space and the RAM is disabled. See 4K Option section (6.3.1) for the necessary hardware changes to convert to 4K EPROMS.

6.3.1 4K EPROM

The MDX-2 may also use the new MCM2532 4K (or equivalent) EPROM's. To enable this option, cut the traces between jumper 17 and jumper 19, and between jumper 20 and jumper 21. Then connect a jumper wire from jumper 17 to jumper 18 and from jumper 21 to jumper 22. These connections tie All into the decode logic and deselect RAM at the upper most 4K of memory (F000-FFFF).

6.4 Power Supply Description

There are four power supplies on the MDX-2, +5,-5,+12 and -12. The user must supply 17.0 VAC and 19.8 VDC to the board. A Radio Shack power pack (RS #4000007) is recommended. If one is not available, a 18 V center-tapped transformer and two 1N4007 diodes can be used. See Fig. 5 for details.

6.4.1 +5 Volts

The 5 volt supply uses CR1 to rectify the 17.0 VAC (also used for -5 volts). This unregulated voltage is filter by C55 and fed to the 78H05 regulator. The 78H05 is a fixed output, 5 amp regular with full thermal overload, short-circuit and safe-area protection. The input and output also have filter capacitors C52 and C53 for high frequency filtering.

6.4.2 -5 Volts

The minus 5 volt supply also uses the raw DC from CR1. It is fed through series limiting resistor R52 to a 5.1 volt zener diode. Filtering is provided by C50 and C53.

6.4.3 +12 Volts

The +12 volt supply uses the 19.8 VDC from the power pack fed through limiting resistor R46 to a 7812 voltage regulator. It is filtered by C23. The output is also filtered by C22.

6.4.4 -12 Volts

The -12 volt supply requires voltage doubling to obtain a negative voltage greater than -15v for regulating. Resistor R45 limits current, and capacitor C19 provides DC blocking. D2 and D3 provide voltage doubling and C20 filters the final doubled unregulated supply (-20 volts). U63 provides the regulated -12 volts which is filtered by C21.

6.5 Real Time Clock Circuit

The Real Time Clock is a 25 millisecond (40hz)interrupt pulse which originates from the divide circuit U17-11. This signal is further divided by U39 and U38. U40a and U40b use this divided pulse to clock U42 whose D input is at ground (logic 0). A read from address 37E0 (hex) is decoded at U41-7. This signal presets U42 forcing a logic 0 at U69-4 and 5. U69 buffers the interrupt to the processor. The 37E0 (hex) decode also enables U55 to clock the pulse through to D6 on the bus. This signal is required because most software available on the market today reads D6 and D7 to identify who gave the interrupt (Real Time Clock or FDC).

6.6 Dual Cassette Circuit

The Dual Cassette option gives the user the ability to control 2 cassette recorders. This option requires an external driver, a TTL gate, a diode and a relay. By toggling bit D0 at address E7E4 (hex), the user can select between cassette one or two.

The following is an example of an assembly program to select the tape machines:

Selecting cassette 1;

```
LDA, 00H                load accumulator A with 00
LD (37E4), A            output accumulator A to U42
```

Selecting cassette 2;

```
LDA, 01H                load accumulator A with 01
LD (37E4), A            output accumulator A to U42
```

The Basic commands for cassette control are CLOAD and CSAVE. To save from cassette 1:

```
CSAVE # - 1, "A"
```

To load from cassette 2:

```
CLOAD # - 2, "A"
```

6.7 Serial Interface

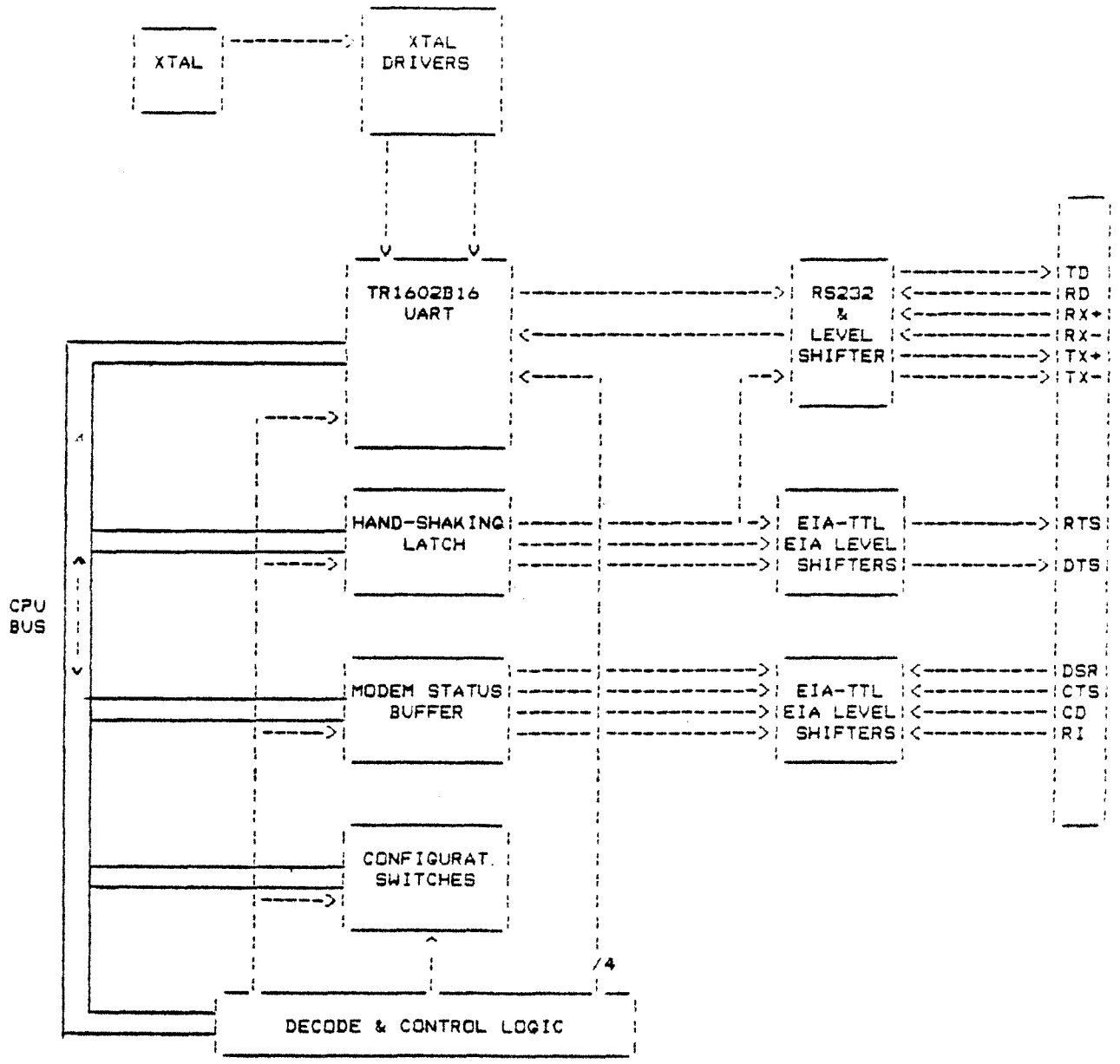
To understand the workings of the MDX-2 Serial Interface, you will need to refer to the schematic and block diagram in Fig. 12. For more information, refer to the TR1602B data sheet in the appendix.

6.7.1 TR1602B UART

The heart of the serial port is the Western Digital Universal Asynchronous Receiver/Transmitter (UART). This part converts the parallel data to serial data for the serial port and receives serial data and converts it to parallel data for the CPU data bus. Two registers are used for read operations --- one for status and the other to hold received data; and two registers for write operations --- one for status and the other for transmit data. Word length, baud, parity, parity inhibit and stop bit generation are selectable by toggle switches (more later).

6.7.2 CRYSTAL AND DIVIDER/DRIVERS

Crystal Y1 is driven by U14 and fed to divider U16 which divides this 4 MHZ clock pulse down for the baud rate control devices U15 and U17. Signals are also taken from this circuit to drive the Real Time Clock and Cassette Interface. The baud rates are controlled by dip switches U28 and U29.



Serial Logic Block Diagram

Fig. 12

6.7.3 HANDSHAKE LATCH

U49 latches data bits D0-D2 when control signal OUT-EAH goes to a logic 0. The outputs of U49 drive two 1488 level converters (U50) for conversion to EIA standard.

6.7.4 MODEM STATUS BUFFER

The modem status buffer U48 is driven by four 1489's (U46) which convert the incoming EIA signals to TTL. The serial input (TTL) is fed to U48-12 which enables the CPU to directly read the serial data.

6.7.5 CONFIGURATION SWITCHES

Dip-Switches U64 enable the configuration of the serial port by enabling the appropriate switch on the CPU data bus when decode signal IN-E9H is a logic 0. All switches are read at one time. They are pulled high and switched low.

6.7.6 DECODE AND CONTROL LOGIC

Decode is accomplished by U43, U44 and U52. These devices give the address decode signals for IN,OUT-E8,E9,EA,EB. U43 and U44 decode address bits A3-A6 (E8) and feed the strobe inputs (U52-2 and U52-14) and A0 and A1 feed the A and B inputs of U52. Data is enabled to the CPU data bus, with a read of either the Receiver Register or the Status Register, by U45 which is enabled by the AND function of IN-EAH and IN-EBH. Fig. 13 is a summary of the address decoding.

IN-E8H - Modem Status Register
IN-E9H - Configuration Switches
IN-EAH - UART Status Register
IN-EBH - UART Received Register, Data Received Reset

OUT-E8H - Master Reset
OUT-E9H - Not Used
OUT-EAH - Load Control Register, Load Handshake Latch
OUT-EBH - Load Transmit Holding Register

Serial Logic Address Decoding

Fig. 13

6.7.7 EIA RS232 AND 20ma LEVEL SHIFTERS AND DRIVERS

The serial output of the UART (U53) is fed through drivers U43 to U54 (20ma interface) and U50 (EIA driver). Serial output is enabled to these devices by U49-10. When U54 conducts, it allows 20ma of current to flow (20ma=mark, 0ma=space). Serial input comes thru U51-1 which converts the signal to TTL. The signal is then sent to the UART (U53) and U48 to be read as part of the Modem Status Buffer. The Phone Modem may be directly read by the Serial Port by inserting jumper wires from jumper 11 to jumper 13 and from jumper 9 to jumper 14.

6.8 PHONE MODEM

Digital transmission uses a Frequency Shift Keying (FSK) modulation scheme. Two frequencies 200 hz apart are used where a logic 1 (mark) is the higher frequency and a logic 0 (space) is the lower frequency of the pair. Two pairs of these frequencies are used for two way communications. This is called Full Duplex operation and is usually limited to 300 baud. The lower pair of frequencies is used for transmission by a terminal while the higher pair is used for receiving. A modem operating in this mode is called an "originate mode" device since a terminal is usually used to originate the call to the computer. "Answer mode" devices operate in just the opposite manner (See Fig. 14).

	ORIGINATE	ANSWER
MARK	1270	2225
SPACE	1070	2025

Modem Operating Frequencies

Fig. 14

A 1 MHZ crystal provides a stable frequency reference. A jumper may be used between pins U57-10, U57-2 and ground to enable the 14412 modem chip to go into the test mode. This will cause a character typed out to appear on the screen. Pin U57-10 controls the mode of operation; a logic 1 is the "originate mode" and a logic 0 on this pin gives the "answer mode". The transmit data output is buffered by U56-2&3 and then mixed with the telephone input by U56-5&6. The purpose of this duplexer is to cancel out the transmit signal to the

filter while amplifying the received signal. U58,59 and 60 and the accompanying resistors and capacitors are 2 three stage filters used to further amplify the signals and reject noise and harmonics. The modem is designed to match the telephone lines 600 ohm impedence by connecting a 1:1 transformer. CONTACT YOUR LOCAL PHONE COMPANY FOR IMFORMATION ABOUT THIS CONNECTION. The output of the 14412 modem chip is jumpered to the serial port for operation by the MDX-2.

6.9 Floppy Disk Controller

The heart of the MDX-2 Floppy Disk Controller (FDC) is the Western Digital FD1771B. This 40 pin I.C. takes care of most of the functions of FDC, including cyclic redundancy checks, internal data/clock separation and all required logging of track location, sector location and I.D. field locations.

The FDC requires a 1 MHZ clock. This clock is provided by the divide-by- two circuit of U39b and U42b, which divide the 4 MHZ clock down to 2MHZ.

Interfacing to the processor is accomplished through an 8 bit data latch and its associated control signals. When reading the FDC, address decoder U41-4 (37ECH READN) will be low enabling U76 and U77 to buffer data from the FDC to the data bus. When writing to the FDC, U41-12 (37ECH WRITEN) is low enabling data to flow from the data bus, through U76 and U77, to the FDC.

Addresses A0 and A1 are internally decoded by the FDC (71) to select read and write operation registers (See Fig. 15). These registers assist the software in controlling the read and write accesses of the FDC.

A0	A1	READ (RE)	WRITE (WE)
0	0	STATUS REG.	COMMAND REG.
0	1	TRACK REG.	TRACK REG.
1	0	SECTOR REG.	SECTOR REG.
1	1	DATA REG.	DATA REG.

FDC Register Selects

Fig. 15

The interrupt request (INTRQ) pin of the FDC (U71-39) indicates the completion or termination of an operation. This interrupt presets flip-flop U42 putting a high on U69-4 and U69-5. This high may be reset by a read of the FDC Status Register. Reading from 37E0 resets the interrupt signal (INT) by clocking a low at the output of U42.

Drive selection is accomplished through data lines D0-D3. These data lines are clocked into U75 by the signal from U41-9 (37E0 write). This signal also triggers U7b-9, a one-shot that turns on the drive motor. Drive selection is only activated when the "drive motor on" signal (U7b-5) is a high. When U7b-5 is low (motor is not on), U75 is cleared and a high is generated at U7-6. This high is inverted by U74 providing a low at U71-23 and U71-32, enabling the FDC.

7.0 Conclusion

You have finally reached the end of this manual. Hopefully (!) you now have a working board that will bring you many hours of enjoyment and enable you to do the things that you anticipated when you entered into this venture. If at any time you have any problems, suggestions, comments or just want to rap, give us a call. We are very interested in your views. We have entered your name on our mailing list (unless otherwise requested) and will be sending you all updates, new modifications and any other material that may be beneficial to you..... So fire it up and ENJOY YOUR MDX-2!!!!!

8.0 APPENDIX

The following is the source to a serial driver program It can be used to test the serial port. To test you must enter the following source and assembly it using the editor-assembler. After assembling the file short together (JP9 to JP11). This ties data out to data in. Load the program and enter FULL DUPLEX. Anything typed on the keyboard will be displayed on the screen.

```
0010 ;
0020 ;                    SERIAL DRIVER
0030 ;                       VER 2.0
0040 ;
0050 ;
0060 ; ENTER ( F ) FOR FULL DUPLEX : HOST WILL ECHO CHARACTERS
0070 ; ENTER ( H ) FOR HALF DUPLEX : HOST DOES NOT ECHO CHARACTERS
0080 ; AFTER ENTERING , DAIL NUMBER AND THROW THE PHONE SWITCH
0090 ;
0100 VIDEO      EQU     33H
0110 KYBD       EQU     2BH
0120 RESET      EQU     0E8H
0130 SWTHES     EQU     0E9H
0140 CONTRL     EQU     0EAH
0150 DATA       EQU     0EBH
0160            ORG     0F800H          ;START
0170 START      CALL    IC9H            ;CLEAR SCREEN
0180            LD      HL,LOGIN        ;GET LOGIN
0190            LD      DE,3C00H+15     ;CENTER ON SCREEN
0200            LD      BC,LOGINL       ;GET LENGTH
0210            LDIR                    ;OUTPUT HERE
0220            LD      HL,MESS         ;GET MESSAGE
0230            LD      DE,3C00H+79     ;CENTER IT
0240            LD      BC,MESSL        ;GET LENGTH
0250            LDIR                    ;OUTPUT HERE
0260            LD      HL,MESSA        ;GET MESSAGE
0270            LD      DE,3C00H+143    ;CENTER IT
0280            LD      BC,MESSAL       ;GET LENGTH
0290            LDIR                    ;OUTPUT HERE
0300            LD      HL,QUES         ;GET QUESTION
0310            LD      DE,3C00H+261    ;CENTER IT
0320            LD      BC,QUESL        ;GET LENGTH
0330            LDIR                    ;OUTPUT HERE
0340            LD      HL,3C00H+310    ;GET CURSER POSITION
0350            LD      (4020H),HL      ;SAVE IT
0360            LD      A,0EH           ;TURN ON CURSER
0370            CALL    VIDEO           ;DISPLAY IT
0380 ANSWER     CALL    KYBD            ;SEE IF ANY KEY
0390            OR      A               ;ANYTHING ?
0400            JR      Z,ANSWER        ;NO ,KEEP LOOKING
0410            CALL    VIDEO           ;YES, DISPLAY IT
0420            CP      46H             ;IS IT " F "
0430            JR      Z,DUPLEX        ;GO IF SO
0440            CP      48H             ;IS IT " H "
0450            JR      Z,DUPLEX        ;GO IF SO
0460            JP      START           ;GO IF NEITHER
0470 DUPLEX     LD      (05000H),A      ;SAVE IT
0480 UART       OUT     (RESET),A       ;RESET UART
```

```
0490             IN      A,(SWTHES)      ;READ SWITCHES
0500             AND     0F8H            ;TAKE OFF LOWER 3 BITS
0510             OR      05H             ;SET JP UART
0520             OUT     (CONTRL),A      ;SAVE IN REG.
0530 RECDA       IN      A,(CONTRL)      ;GET REG.
0540             BIT     7,A             ;HAS IT CHANGED ?
0550             JR      Z,URTOUT        ;NO , GO TO OUTPUT
0560             IN      A,(DATA)        ;YES , GET DATA
0570             OR      A               ;ANYTHING ?
0580             JR      Z,URTOUT        ;NO , GO TO OUTPUT
0590             AND     7FH             ;YES , REMOVE PARITY
0600             CP      60H             ;IS IT PRINTABLE ?
0610             JP      M,NOLWER        ;YES , PRINT IT
0620             AND     5FH             ; NO , CONVERT IT
0630 NOLWER      CP      0AH             ;IS IT LINEFEED ?
0640             JR      Z,RECDA         ;GO TO RECIEVE DATA
0650             CALL    VIDEO           ;DISPLAY IT
0660             JP      RECDA           ;GO TO REICIVE DATA
0670 URTOUT      CALL    KYBD            ;GET KEYBOARD
0680             OR      A               ;ANYTHING ?
0690             JR      Z,RECDA         ;GOTO RECIEVE DATA
0700             CP      01H             ;IS IT BREAK KEY ?
0710             JR      Z,BREAK         ;YES , GOTO BREAK
0720             CP      64H             ;IS IT SHIFT D
0730             JR      Z,EOF           ;YES , GOTO (EOF)
0740 OUTDA       LD      C,A             ;SAVE IT
0750             IN      A,(CONTRL)      ;GET STATUS
0760             BIT     6,A             ;IS REG. EMPTY ?
0770             JR      Z,OUTDA         ;KEEP TRYING
0780             LD      A,C             ;PUT CHARACTER IN A
0790             OUT     (DATA),A        ;SEND IT OUT
0800             LD      A,(05000H)      ;PUT IN DUPLEX
0810             CP      048H            ;IS IT HALF DUPLEX ?
0820             JR      NZ,RECDA        ;GO IF FULL DUPLEX
0830             LD      A,C             ;GET CHARACTER
0840             CALL    VIDEO           ;PUT ON SCREEN
0850             JP      RECDA           ;GOTO RECIEVE DATA
0860 BREAK       LD      A,7FH           ;PUT IN (INT)
0870             JP      OUTDA           ;SEND IT OUT
0880 EOF         LD      A,04H           ;PUT IN (EOF)
0890             JP      OUTDA           ;SEND IT OUT
0900 QUES        DEFM ' ENTER ( F ) FOR FULL ... ( H ) FOR HALF DUPLEX '
0910 QUESL       EQU     $-QUES
0920 LOGIN       DEFM ' SERIAL  DRIVER  PROGRAM '
0930 LOGINL      EQU     $-LOGIN
0940 MESS        DEFM '   BY : MICRO-DESIGN'
0950 MESSL       EQU     $-MESS
0960 MESSA       DEFM '          VER  2.0 '
0970 MESSAL      EQU     $-MESSA
0980 ;
0990             END     0F800H          ; END OF START
```

The following is the opcode table for the Serial Program. You can use TBUG to insert the program if you can not assembly the source listed above.

```
F800  CD C9 01 21 D6 F8 11 0F 3C 01 1F 00 ED B0 21 F5
F810  F8 11 4F 3C 01 15 00 ED B0 21 0A F9 11 8F 3C 01
F820  13 00 ED B0 21 A7 F8 11 05 3D 01 2F 00 ED B0 21
F830  36 3D 22 20 40 3E 0E CD 33 00 CD 2B 00 B7 28 FA
F840  CD 33 00 FE 46 28 07 FE 48 28 03 C3 00 F8 32 00
F850  50 D3 E8 DB E9 E6 F8 F6 05 D3 EA DB EA CB 7F 28
F860  17 DB EB B7 28 12 E6 7F FE 60 FA 6F F8 E6 5F FE
F870  0A 28 E8 CD 33 00 18 E3 CD 2B 00 B7 28 DD FE 01
F880  28 1B FE 64 28 1C 4F DB EA CB 77 28 F9 79 D3 EB
F890  3A 00 50 FE 48 20 C4 79 CD 33 00 18 BE 3E 7F C3
F8A0  86 F8 3E 04 C3 86 F8 45 4E 54 45 52 20 28 20 46
F8B0  20 29 20 46 4F 52 20 46 55 4C 4C 20 2E 2E 20 28
F8C0  20 48 20 29 20 46 4F 52 20 48 41 4C 46 20 44 55
F8D0  50 4C 45 58 20 2E 53 45 52 49 41 4C 20 44 52 49
F8E0  56 45 52 20 46 4F 52 20 54 48 45 20 4D 44 58 20
F8F0  4D 4F 44 45 4D 20 20 42 59 20 3A 20 20 20 4D 49
F900  43 52 4F 2D 44 45 53 49 47 4E 20 20 20 20 20 20
F910  20 20 20 20 20 56 45 52 20 20 32 2E 30 00 00 00
```

After entering, use the punch command to save the program to tape.

EXAMPLE: TBUG COMMAND

```
P F800 F91F F800 SERIAL
```

C O R P O R A T I O N

TR1602/TR1402/TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

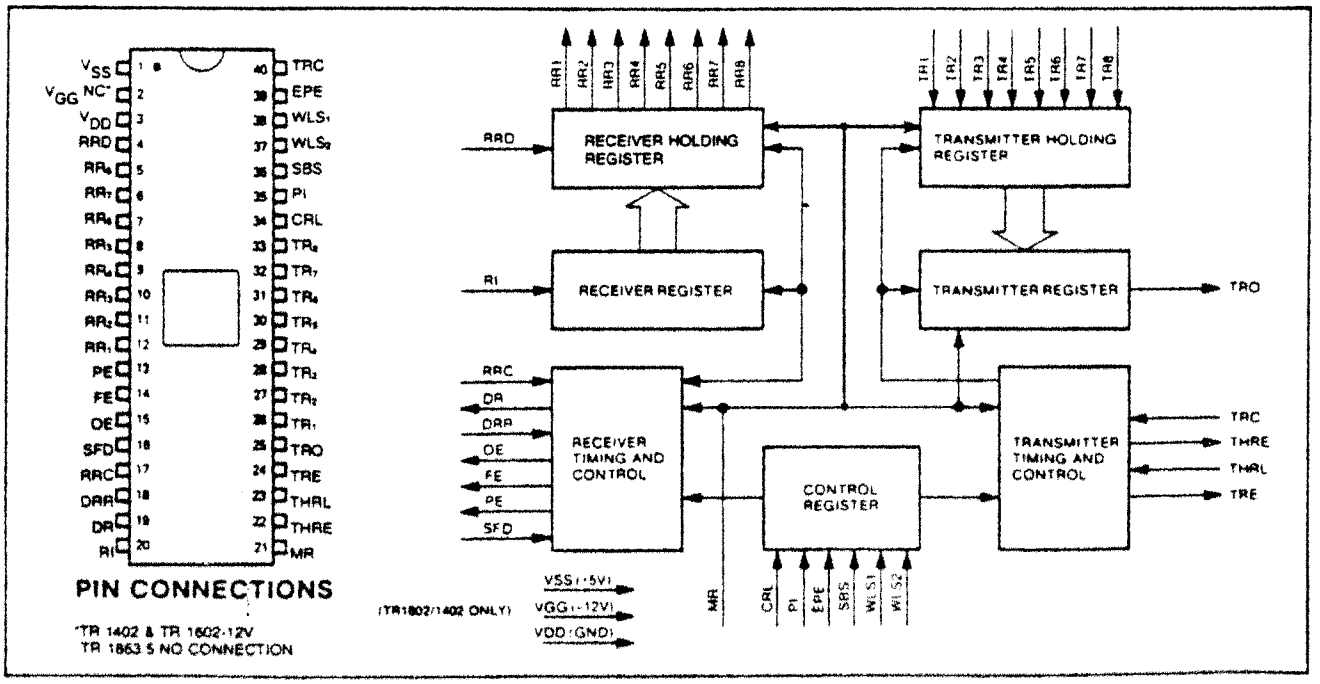
AUGUST, 1980

FEATURES

- DUAL POWER SUPPLY TR1602/TR1402
- SINGLE POWER SUPPLY — +5VDC ON TR1863/5
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  - Word Length
  - Baud Rate
  - Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  - Parity Inhibit
  - One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level for TR1602,TR1863/5)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  - Transmission Complete
  - Buffer Register Transfer Complete
  - Received Data Available
  - Parity Error
  - Framing Error
  - Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  - Receiver Register Outputs
  - Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



TR1602/TR1402/TR1863/TR1865 BLOCK DIAGRAM

GENERAL DESCRIPTION

The ASYNCHRONOUS RECEIVER TRANSMITTER is a general purpose, programmable MOS, LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start/stop bits, and optional parity. The receiver section converts a serial word with start, data, optional parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffere The array is compatible with bipolar logic. The arr may be programmed as follows: The word length c be either 5, 6, 7, or 8 bits; parity generation and chec ing may be inhibited, the parity may be even or oc and the number of stop bits may be either one or tw with one and one-half when transmitting a 5 bit coc The TR1863/5 is pin- and function-compatible to t TR1402 and TR1602 except that it is −5V only a can operate up to 3.5 MHz (218.75K Baud). The sta dard TR1863/5 operates at 1.0 MHz (62.5K Bau (NOTE: See TR1402A Data Sheet for operation w 5-level code-2 stop bits.)

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	VSS	-5 volts supply
2	V_{GG} — TR1602/TR1402 NC — TR1863/5	V_{GG} NC	-12 volts supply No Connection (open)
3	V_{DD} POWER SUPPLY	GND	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR8RR1 data outputs (pins 5-12)
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected

PIN NUMBER	NAME	SYMBOL	FUNCTION
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times times the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Holding Registers, the Transmitter Register, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REIGSTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage VOH, to a low-level output voltage, V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_2 and WLS_2), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.

PIN NUMBER	NAME	SYMBOL	FUNCTION
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1602 and TR1863 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WORD LENGTH SELECT	WLS_2 -WLS_1	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

WESTERN DIGITAL
CORPORATION

FD1771-01 Floppy Disk Formatter/Controller

FEATURES

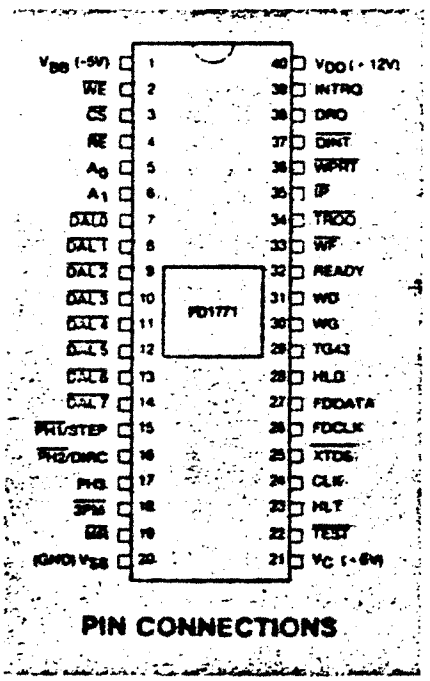
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- READ MODE
  - Single/Multiple Sector Write with Automatic Sector Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- PROGRAMMABLE CONTROLS
  - Selectable Track-to-Track Stepping Time
  - Selectable Head Settling and Head Engage Times
  - Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8-Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible

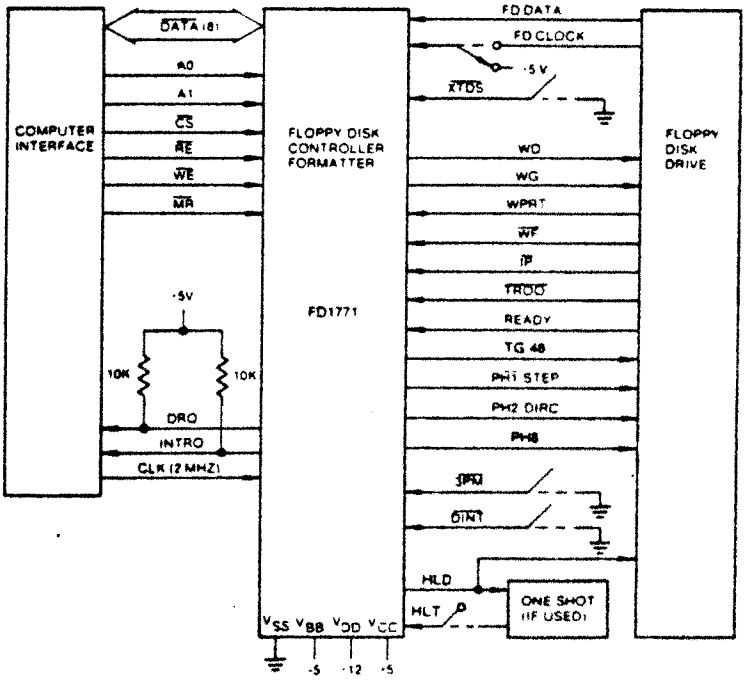
APPLICATIONS

- FLOPPY DISK DRIVE INTERFACE
- SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
- NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface





FD1771 SYSTEM BLOCK DIAGRAM

organization that accommodates the interface signals from most drive manufacturers. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The A and B suffixes are for ceramic and plastic packages, respectively.

PIN OUTS

Pin No.	Pin Name	Symbol	Function
1	Power Supplies	V_{BB}/NC	-5V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high, a Restore Command is executed, regardless of the state of the Ready signal from the drive.
20		V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
Computer Interface			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A_0, A_1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A_1 A_0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Register Command Register 0 1 Track Register Track Register 1 0 Sector Register Sector Register 1 1 Data Register Data Register
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
24	CLOCK	CLK	This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
Floppy Disk Interface:			
15	Phase 1/Step	$\overline{PH1}$/STEP	If the $\overline{3PM}$ input is a logic low the three-phase motor control is selected and $\overline{PH1}$, $\overline{PH2}$, and PH3 outputs

Pin No.	Pin Name	Symbol	Function
16	$\overline{\text{Phase 2}}$/Direction	$\overline{\text{PH2}}$/DIRC	form a one active low signal out of three. $\overline{\text{PH1}}$ is active low after $\overline{\text{MR}}$. If the $\overline{\text{3PM}}$ input is a logic high the step and direction motor control is selected. The step output contains a 4 usec high signal for each step and the direction output is active high when stepping in; active low when stepping out.
17	Phase 3	PH3	
18	$\overline{\text{3-Phase Motor Select}}$	$\overline{\text{3PM}}$	
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user.
23	HEAD LOAD TIMING	HLT	The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
25	$\overline{\text{EXTERNAL DATA SEPARATION}}$	$\overline{\text{XTDS}}$	A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	This input receives the externally separated clock when $\overline{\text{XTDS}}$ = 0. If $\overline{\text{XTDS}}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	This input receives the raw read disk data if $\overline{\text{XTDS}}$=1, or the externally separated data if $\overline{\text{XTDS}}$=0.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	Track Greater than 43	TG43	This output informs the drive that the Read-Write head is positioned between tracks44-76. This output is valid only during Read and Write commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
31	WRITE DATA	WD	This output contains both clock and data bits of 500 ns duration.
32	Ready	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low, the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	This input detects wiring faults indications from the drive. When WG=1 and $\overline{\text{WF}}$ goes low, the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write command is received. A logic low terminates the command and sets the Write Protect status bit.
37	$\overline{\text{DISK INITIALIZATION}}$	$\overline{\text{DINT}}$	The iput is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$=0, the operation is terminated and the Write Protect status bit is set.

Warranty

Your Micro-Design P.C. board is warranted against defects for a period of 60 days from the date of delivery. We will repair or replace products that prove to be defective during the warranty period provided they are returned to Micro-Design.

A service charge will incure on repairs where Micro-Design is not at fault. No other warranty is expressed or implied. Micro-Design is not liable for consequential damages.

Helpful Hints

* If your memory fails to operate properly, install capacitors C52 and C53 (2200 pfd).

* If your floppy does not boot-up, check to be sure that U14 is a 74s04 (not a 74ls02). Also, you must have at least 32K of memory for the floppy controller to operate (memory passes memory test)

* If you have problems with your modem due to phone line noise, add resistance to R22 up to 600 ohms.

* Below is a very simple, yet very good memory test. Load it in basic and run it. If memory is good, it will stay in a loop counting down from the top of memory. If it quits counting down, the location it stops at is bad.

```
10 CLS:PRINTCHR$(32)
20 PRINT@467,MEM: IF MEM <100 THEN RUN ELSE GOSUB10
30 END
```

* IF AT ANYTIME YOU HAVE A PROBLEM, PLEASE DROP US A LINE OR GIVE US A CALL. WE WILL HELP IN ANYWAY POSSIBLE TO SATISFY YOU WITH OUR PRODUCTS.

Micro-Design
P.O. Box 748
Manchaca, Texas 78652
(512) 282-0225

The following parts supply houses carry the parts required for the MDX boards. These suppliers each carry MOST of the parts required, but no one particular supplier has all the parts. If you have any problems finding parts,(or need to know exactly who has what part), please let us know and we will gladly help you acquire the parts you have problems finding. Our 24 hour number is 1-512-4582937.

For quicker, more reliable service, mention MICRO-DESIGN!

Austin Electronics
1536 E. Anderson Lane
Austin, Texas 78752
(512) 836-9677

K.A. Electronics
8910 Research Blvd.
Austin, Texas 78758
(512) 458-2257

Wholesale Electronics
507 Pressler St.
Austin, Texas 78701
(512) 478-9568

Jameco Electronics
1355 Shoreway Road
Belmont, Ca. 94002
(415) 592-8097

MD
MICRO-DESIGN

INTERFACE EXPANSION BOARD

RAM

EPROM

LINE PRINTER

REAL-TIME CLOCK

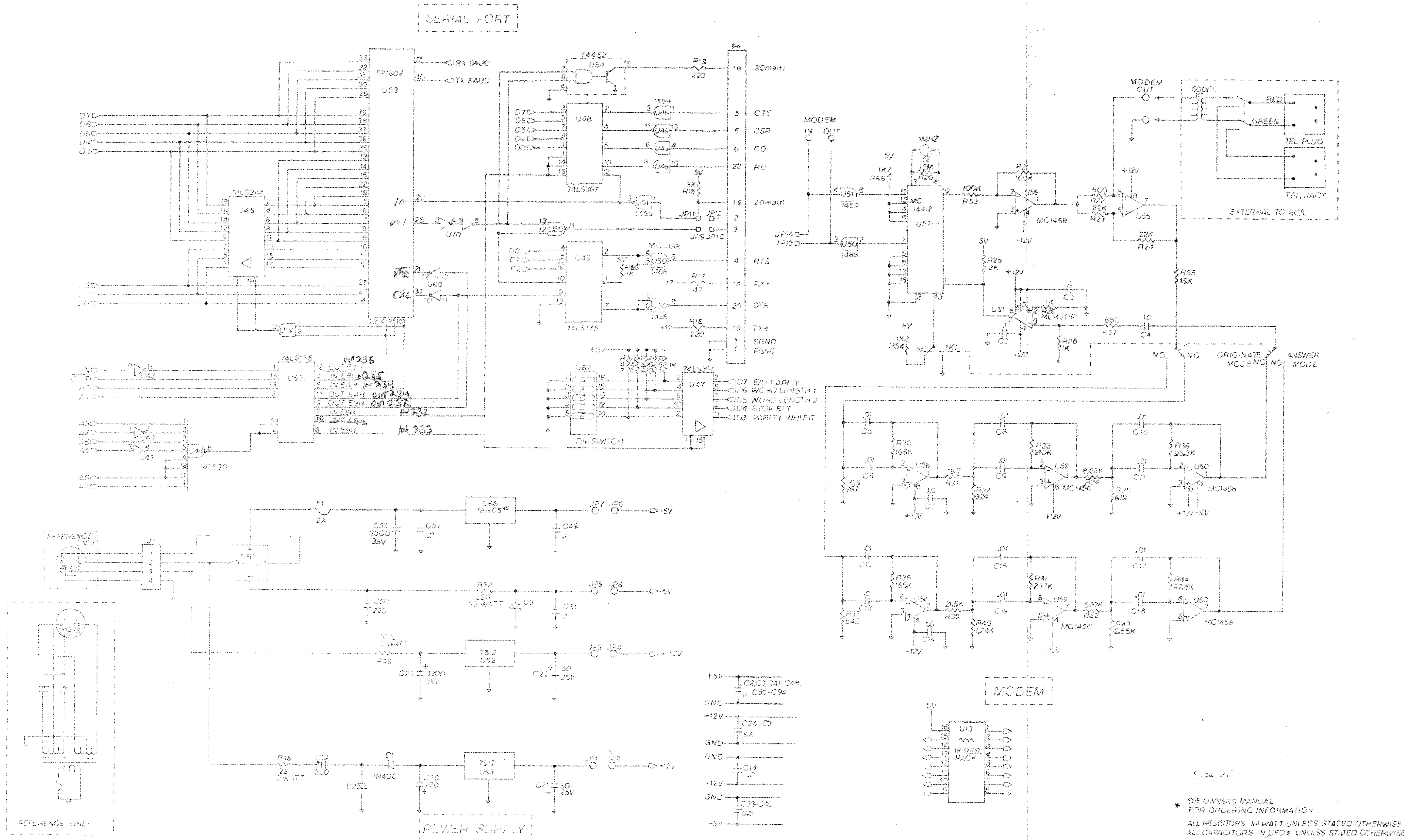
MINI DISK BUS

GROUND PINS:
2,4,6,8,10,12,14,16,18
20,22,24,26,27,31,33,34

FAULT
UNIT SELECT
PAPER OUT
BUSY
DATA STROBE

MOTOR ON
STEP
DIRECTION
WRITE GATE
WRITE DATA
READ DATA
WRITE PROTECT
INDEX SELECT
TRACK ZERO

ALL ODD PINS GND


SERIAL PORT
MODEM
POWER SUPPLY
REFERENCE ONLY
EXTERNAL TO RCR.
TEL PLUG
TEL JACK
ORIGINATE MODE
ANSWER MODE
DIP SWITCH
E/O PARITY
WORD LENGTH 1
WORD LENGTH 2
STOP BIT
PARITY INHIBIT
* SEE OWNERS MANUAL FOR ORDERING INFORMATION
ALL RESISTORS 1/4 WATT UNLESS STATED OTHERWISE
ALL CAPACITORS IN μFD's UNLESS STATED OTHERWISE