LINE	PART NUMBER	QTY.	
1	MS-2604153	1	GAVAG FF 26.82 +TAX OC 821408

Radio Shack®

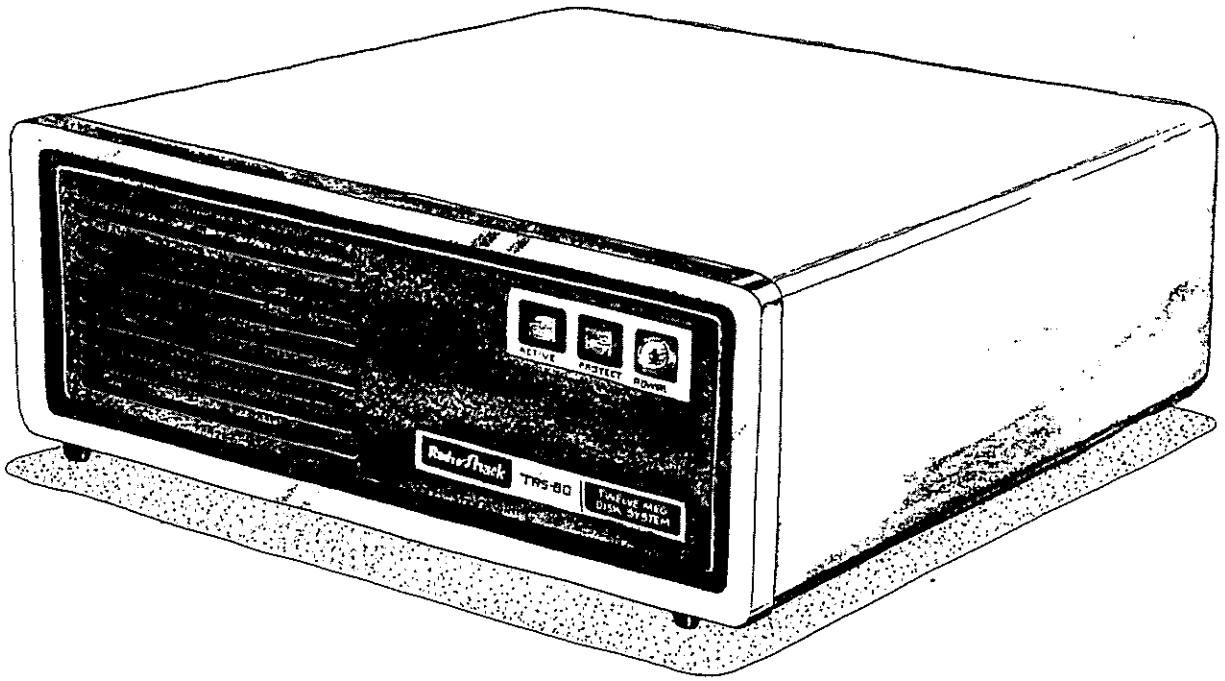
Service Manual

26-4152/3/5/6

TRS-80®

12/15 Meg Hard Disk

Catalog Numbers 26-4152/3/5/6



CUSTOM MANUFACTURED IN U.S.A. BY RADIO SHACK, A DIVISION OF TANDY CORPORATION

TRS-80®

TRS-8Ø® 12/15 Meg Hard Disk

Service Manual

Catalog Number 26-4152/3/5/6

Radio Shack®

TRS-80®

TRS-8Ø® 12/15 Meg Hard Disk Service Manual

Radio Shack®

Contents

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Warnings

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Do not move or tilt the Hard Disk Drive unit while the drive is running. Permanent damage to the drive may occur resulting in the loss of information or damage to the disk.

Do not drop the Hard Disk Drive unit from any height as permanent damage to the drive may occur.

1/ Overview

The Disks and Read/Write heads are fully enclosed in a sealed chamber. A special air filteration system prevents dust and other particles, which destroy data, from reaching the disks. Another filtering system allows pressure equalization with the "outside" air pressure.

UNDER NO CIRCUMSTANCES MUST THE CHAMBER BE UNSEALED IN THE FIELD. A CLASS 1ØØ CLEAN ROOM ENVIRONMENT IS NEEDED FOR UNDER-THE-BUBBLE REPAIR.

CAUTION notes about disassembly of the bubble pack contained in the 12/15 Meg Hard Disk Drive manual are applicable to both units.

On all Hard Disk Units, flaws in the media are indentified at the factory before the disk drives are delivered to the customer. Attached to the bottom of each disk drive unit is a "Media Error Map". This map identifies the flawed tracks on that particular unit.

Most of the information contained in the 12/15 Meg Hard Disk manual is applicable to either unit with the exception of references in the Technical Specifications section and the addition of the 15 Meg Hard Disk parts list. Specifications are different for each Unit. Mechanically, the two units are identical except for the disk drive unit bubble.

2/ Technical Specifications (12 Meg)

Basically, the hard disk unit consists of three platters (or disks) lying parallel within the unit. There are also six Read/Write heads, one on each side of each platter. These heads move towards or away from the center of the disk as needed.

When a unit is purchased, there will be no more than 3 tracks per head with defects. This will not exceed 8 tracks per drive with defects. Also there will not be any flaws on Track Ø.

Technical Specifications (12 MEG)

Disks/Platters	3
Heads/Recording Surfaces	6
Tracks per Inch	254
Cylinders	23Ø
Tracks	138Ø

Hard Disk	Cylinders	Tracks	Sectors	Bytes
1	23Ø	138Ø	46,92Ø	12,Ø11,52Ø
---	1	6	2Ø4	52,224
---	---	1	34	8,7Ø4
---	---	---	1	256

Technical Specifications (15 meg)

Disks/Platters	3
Heads/Recording Surface	6
Tracks per Inch	345
Cylinders	3Ø6
Tracks	1836

For drives formatted with 256 bytes/sector:

Hard Disk	Cylinders	Tracks	Sectors	Byte
1	306	1836	58,752	15,040,512
-----	1	6	192	49,152
-----	---	1	32	8,192
-----	---	---	1	256

For drives formatted with 512 bytes/sector:

Hard Disk	Cylinders	Tracks	Sectors	Byte
1	306	1836	31,212	15,980,544
-----	1	6	102	54,244
-----	---	1	17	8,704
-----	---	---	1	512

Hard Disk Drive 15 Meg

Disk Organization

Tracks per Unit	1,836
Tracks per Platter	612
Sectors per Track	32 or 17
Bytes per Sector	256 or 512
Cylinders per Disk	306
Average Latency	8.34 msec
Rotational Speed	3,600 rpm +/- 1%
Recording Density	9,090
Flux Density	9,090
Track Density	345 TPI

Storage Capacity

Unformatted

Bytes per Track	10,400
Bytes per Surface	3.19 Meg
Bytes per Drive	19.14 Meg

Formatted

Bytes per Drive	15 Meg (Primary and Secondary)

Hard Disk Drive 12 Meg		
Disk Organization		
Tracks per Unit	138Ø	
Tracks per Platter	46Ø	
Sectors per Track	34	
Bytes per Sector	256	
Cylinders per Disk	23Ø	
Average Latency	8.34	msec
Rotational Speed	36ØØ	rpm +/- 1%
Recording Density	9625	
Flux Density	9625	
Track Density	254	
Storage Capacity (Hard Disk)		
Unformatted		
Bytes per Track	1Ø4ØØ	
Bytes per Surface	2.39	MEG
Bytes per Drive	14.35	MEG
Formatted		
Bytes per Drive	12 M (Primary)	
	12 M (Secondary)	

Specifications for 12 and 15 Meg

Dimensions		
Height		5.5 in (14Ø mm)
Width		14. in (356 mm)
Length		15. in (381 mm)
Weight		
	Primary	15.5 lbs (7.Ø2 kg)
	Secondary	12.5 lbs (5.68 kg)

Environment	
Ambient Temperature	5Ø to 95 degrees F. (1Ø to 35 degrees C.)
Relative Humidity	8% to 8Ø%
Maximum Wet Bulb Temp.	78 F. (26 C.) non-condensing
Heat Dissipation	15Ø Watts (511 BTU/Hr)
Altitude	operating: Ø to 6ØØØ feet (Ø to 1829 meters) storage: Sea Level to 12ØØØ feet (Ø to 3656 meters)

Warm-Up Period	
Minimum On Power-Up	2 minutes
Minimum to Turn System On After Turning System Off	15 seconds

AC Power Requirements

5Ø/6Ø Hz
1ØØ/115 VAC installations (9Ø to 127 V)
2ØØ/23Ø VAC installations (2ØØ to 253 V)
Fuse 2.5 Amps at 25Ø Volts (Internal)

3/ Interface Board Installation

Models II and 16/16B

Install the 5Ø pin connector in the back panel of the computer (below the disk expansion connector).

Connect (jumper) pins AK-AP, A-B, A-B, V-W on the Interface Board.
NOTE: There are two sets of A-B jumpers.

Insert the Interface Board.

Connect the internal cable from the connector on the interface board to the 5Ø pin connector on the back panel of the computer..

Change R21 (15Ø ohm) and boot ROM. Also modify Z8Ø CPU board per technical bulletin II:26 (Enhanced DMA Mod.)

Model 12

In order to install the interface board in the Model 12 the card cage must be installed first (see - Seven Slot Expansion Kit Instructions - 26-6Ø17).

Connect (jumper) the following pins on the Interface Board.

Model 12 AG-AL, A-B, A-B, V-W.

Insert the Interface Board.

4/ Connections

Connecting Your Primary Drive

Be sure all power is OFF.

Note: The Master (Primary) unit does not come with Data Out connectors. These are supplied with each secondary unit and require installation.

Models II and 16

Connect one end of the hard disk expansion cable to the 5Ø pin connector on the back of the computer.

Connect the opposite end of the hard disk expansion cable to the COMPUTER IN connector, located on the rear panel of the primary drive.

Model 12/16B

Locate the hard disk expansion cable. Connect one end of the cable to the Interface card connector of your Model 12 or 16. Be sure the cable exists the rear of the computer so that it won't bind.

Connect the opposite end of the hard disk expansion cable to the COMPUTER IN connector, located on the rear panel of the primary drive.

Connect the power cord to the primary drive. Plug the other end into an appropriate AC power source.

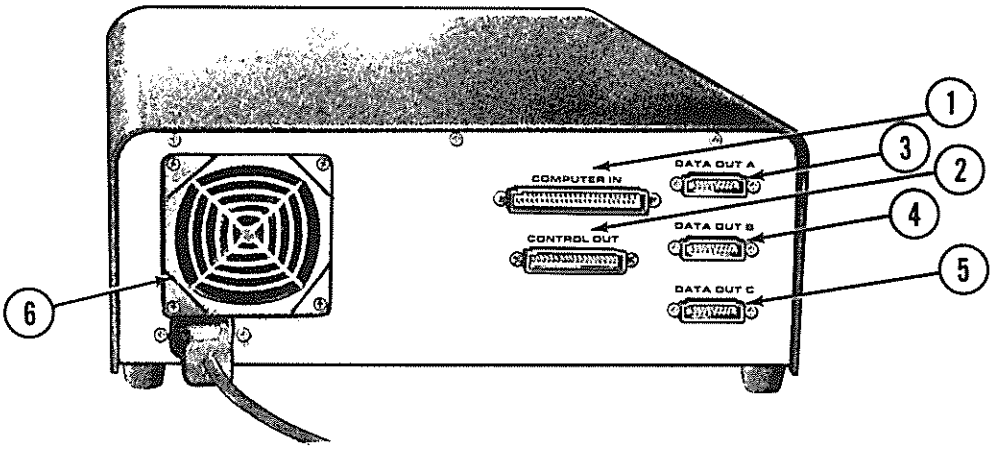


Figure 1. Back Panel of Hard Disk Drive

1. Computer In (5Ø-pin) Connect the Hard Disk Expansion Cable from the Computer to this connector.

2. Control Out (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this connector. The other end connects to the first secondary drive.

3. Data Out A (2Ø-pin) Connect one end of the Data Cable from the first secondary drive to this connector.

4. Data Out B (2Ø-pin) Connect one end of the Data Cable from the second secondary drive to this connector.

5. Data Out C (2Ø-pin) Connect one end of the Data Cable from the third secondary drive to this connector.

6. Filter

Connecting Secondary Drives

The secondary drives are connected to the computer via the primary disk drive. The drives must be stacked with the primary drive on top of the secondary drives.

Locate the secondary hard disk expansion cable. Connect one end to the Control In connector of the secondary drive and the other end to the Control Out connector of the previous drive in the chain. If you have only two hard disk drives, this connector connects to the primary drive.

If you have another secondary drive, connect the second secondary hard disk expansion cable to the Control Out connector and the other end to the Control In connector of the next drive in the chain.

Locate the data cable. Connect one end to the appropriate data connector (A for the first secondary drive, B for the second, and C for the third). Connect the other end to the Data In connector on the secondary drive.

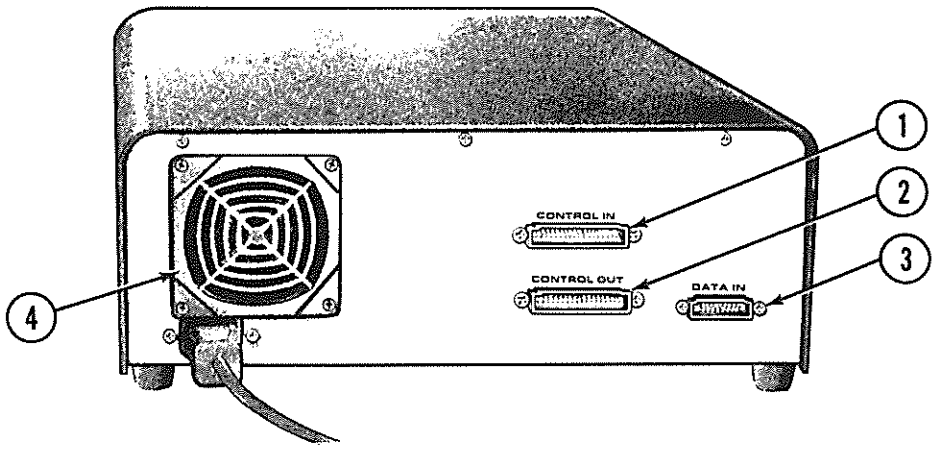


Figure 2. Back Panel of Secondary Hard Disk Drive

1. Control In (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this connector. The other end connects to the previous Hard Disk Drive.

2. Control Out (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this connector. The other end connects to the next secondary drive.

3. Data In (2Ø-pin) Connect one end of the Data Cable from the the primary drive to this connector.

4. Filter

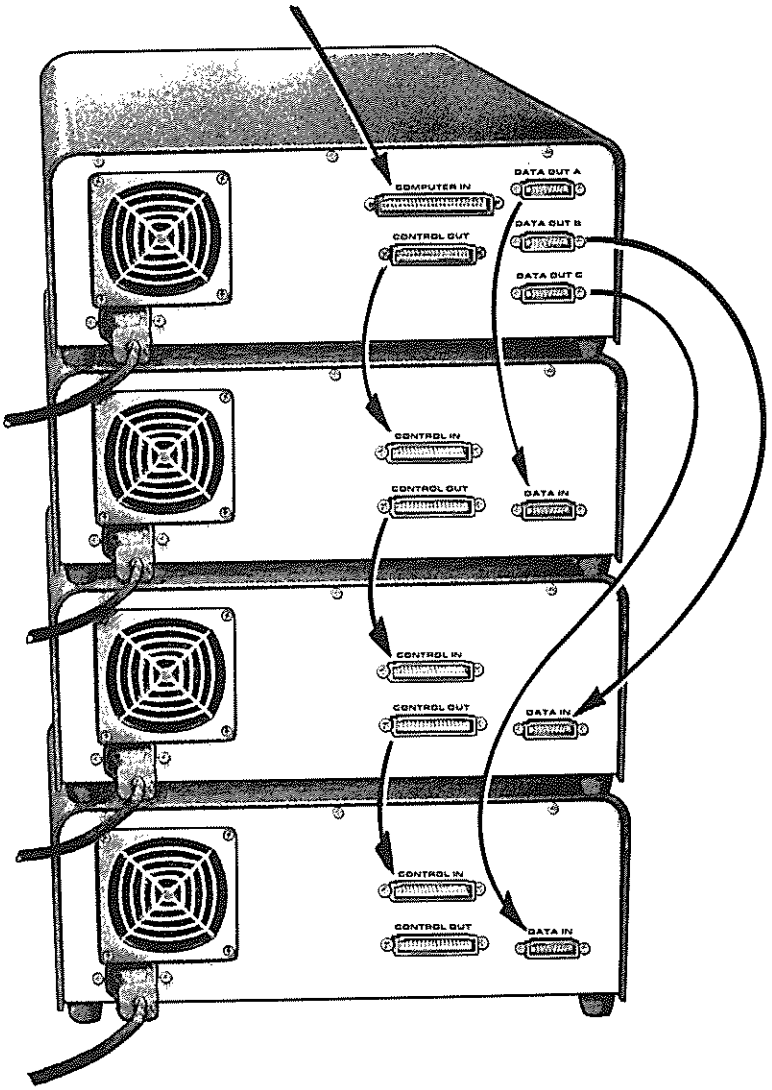


Figure 3. A Fully Configured Hard Disk System

5/Power-Up and Power-Down

System Power-Up

1. Make sure all power is OFF and all floppy diskette drives are empty.

2. Turn on all peripheral equipment (such as a printer or additional floppy diskette drives)

3. Turn on the primary hard drive by turning the POWER KEY clockwise. This also turns on all secondary drives. All secondary drives' power lights should come on.

4. Turn the computer ON.

5. Insert either the FORMAT diskette or the START-UP diskette in floppy Drive Ø.

6. Press RESET. In a few seconds the screen shows a large TRSDOS II logo.

   If the TRSDOS II logo does not appear, repeat the above steps, making sure you inserted the diskette properly. It may be necessary to hold the [Break] and [Repeat] key to boot floppy.

7. The screen then shows this prompt:

   TRSDOS II Ready

   Since you've not yet initialized your Hard Disk System, the computer is now operating as a Floppy Disk System, the only way it can operate until you initialize it.

   If you've initialized the Hard Disk System, you can remove the START-UP diskette. You only need it to start up or reset.

To operate the system for floppy disk only, hold down the <CLEAR> key and press the RESET button. (You must keep the <CLEAR> key down until TRSDOS II Ready appears.)

System Power-Down

1. The TRSDOS II Ready prompt should be the last line on your screen. If not, press <ENTER> or exit your program so that it appears.

2. Remove all floppy diskettes from their drives.

3. Turn off the hard disk drive by turning the power key on the primary drive counterclockwise. This turns off all the drives.

4. Turn off any peripheral equipment.

5. Turn off the computer.

6/ Replacement Procedures

Replacement procedures contained in this manual are limited to case disassembly, removal and replacement of subassemblies, and case assembly.

Before beginning repair, disconnect all external cables from the rear connector panel.

Disassembly

1. Remove the top row of screws (3) from the rear panel and lift off the case.

2. To remove the hard disk controller board, remove all cables from the board (data cables, hard disk expansion cable, controller connecting cables, power harness, and lamp controller harness).

NOTE: At the time of disassembly, be sure that the nylon washer on center stand-off is saved for reassembly.

3. To remove the hard disk power supply, remove the 4 screws which secure the power supply mount-and-shield to the bottom of the unit and lift off the cover. Loosen all cables. Disconnect the power harness from the drive unit. Remove the six screws which hold the power supply board.

Reassembly

1. Fasten the power supply in the bottom of the unit by using 4 #6 screws and 2 #1Ø screws. Reconnect the power cables.

2. Replace the power supply shield-and-mount and fasten it using 4 #6 screws. Reconnect the power harness on drive. Position the clear insulating sheet on the power supply mount-and-shield.

3. Be sure and replace nylon washer between the hard disk controller board and center stand-off. Fasten the board using five #6 screws.

4. Reconnect all cables, the lamp driver harness, and the power harness. (Make sure that the lamp driver harness is toward the rear of the unit.) Be sure that the data cables are connected so that the cable comes from the left-hand side of the plug when looking from the front of the unit.

5. Replace the case top and 3 #6 screws in the rear panel.

Note: If you have plated media be sure you have the correct logic board.

7/ Maintenance

The only regular maintenance the 12-Meg Disk Drive requires is a periodic cleaning of the filter on the back of the unit. Clean this filter whenever it becomes filled with dust and particles.

To clean the filter, carefully remove the outer grill -- DO NOT REMOVE THE SCREWS. Then remove the filter and rinse with tap water. When the filter is completely dry, put it back in the drive.

8/ Theory of Operation

Interface Board

Features

- Standard Model II Bus Interface
- On Board CTC For Interrupt Control
- DMA Operation Capability
- Internal 16K Dynamic RAM
- Handles Up To 4 Disk Drives

Signal Interfacing to Model II Bus

Data is passed betweeen the interface board and the Model II type system bus via one 83Ø3 transceiver, U4Ø. Address and control signals are taken off the system bus and buffered by two LS24Ø inverting drivers. U42 carries the address lines and U43 carries the control signals. Also two signals are driven onto the system bus by U39, using two of its four open collector output nand gates. These two Model II signals are WAIT* and XFERRQ*. All of the above signals lead to Jl, an 8Ø pin edge connector which plugs into a standard Model II type mother board.

Signal Interfacing to Hard Disk Controller Bus

Data is transfered to the HDC bus in the same manner as to the Model II bus using one 83Ø4 non-inverting transceiver, Ul3. Address lines AØ through A7 are driven onto the HDC bus by Ul4, an LS244 non-inverting buffer. Another LS244 driver, Ul5, is used to supply the HDC bus with all necessary control signals as well as suppling the following signals to the interface board from the HDC; HDBWAIT*, HDBINTRQ*, and HDBSEL*. HDBSEL* is used as a direction switch for the interface to HDC data bus.

All communication between the interface board and the external HDC is done through J2, a 5Ø position right angle pin header. A ribbon cable leads from J2 on the board to a 5Ø pin I/O header mounted on the back panel just below the connector for the floppy disk expansion bay.

Port Decoding Logic

The hard disk has 16 port mapped addresses for control and ID registers. A jumper setting (A to B for ports CØ-CF) is used to determine the addresses to be decoded as an access to the HDC. The hard disk for the Model II is mapped from CØ to CF HEX. Other port ranges may be selected via this jumper scheme. However, existing software is intended only for use in the CØ-CF ports.

U28, a 74S138, is used to decode the upper nibble of the port byte address. There are four outputs available from U28, each corresponding to a group of 16 port addresses. Selection of the port range is done by means of a single jumper as mentioned above. The following are jumper options for these port range options: A-B (CØ-CF HEX); A-C (7Ø-7F HEX); A-D (6Ø-6F HEX); A-E (5Ø-5F HEX). The selected output signal at A is the enable for one-half of U3Ø, a 74S139 two into four decoder. U3Ø uses address lines A2 and A3 to give the outputs SELDCR* (select device control register), CTCCE* (CTC chip enable), or SELDIR* (select device ID register).

CTCCE* is gated with DEVEN to form the signal CTCCS* which when active low indicates an access of the on-board CTC.

SELDIR* is also gated with WRID* by U23 and tied to the enable of one-half of U3Ø. Only one of the four outputs is used and that is called WRDIR1* which when active low indicates a write operation to port C1. This signal latches the data bus onto the outputs of U35. This 74LS273 latch is used to provide the following signals to the interface board: DEVEN, INTRQEI, DMAEI, and SFTINT.

U38, a 74S64, is a multiple input AND-OR-INVERT gate. The output of this after being inverted again by one-sixth of U31 is used to enable the bus transceivers to either write data to or read data from the Model II bus. This signal is called M2DEN and when active (high) data is written to the system bus from the interface board.

CTC

The Z8Ø CTC (U22) on the interface board provides the Model II with an interrupt vector for up to four interrupting conditions from the hard disk contoller. CTC channels Ø to 3 are port mapped from locations C4 to C7 respectively (when using port ranges CØ-CF). The CTC uses the standard Z-8Ø system interrupt protocol where interrupt priorty is determined by a peripheral device's location in the daisy chain. Because of this there cannot be an open card slot on the Model II mother board between the CPU board and the interface board.

16K Dynamic RAM

The 16K bank of memory on the interface board is set up the same as the memory on the Model II memory board. This RAM is jumpered to replace locations 8ØØØH to BFFFH, bank F of the standard memory board's RAM.

For a detailed description of the memory address and data decoding see the Model II Technical Reference Handbook (#26-4921).

INTRODUCTION TO HARD DISK CONTROLLER

All 12 Meg Hard Disks were shipped with the 8X3ØØ based controller boards. However, the 15 Meg Hard Disks may have the 8X3ØØ or the new WD1Ø1Ø based controller board. The new board, designated the WD1ØØØ-TB1, is easy to recognize because it is approximately one-half the size of the 8X3ØØ based controller. These two controllers are functionally equivalent, however certain versions of software are not compatible between the two.

Controller Board - 8X3ØØ Based

General

The hard disk controller board is a discrete implementation of all functions required to control the 5.25 inch disk drive via a standard data and control bus. The controller is fabricated using a mix of high-speed bipolar and NMOS devices contained on a single two-sided PC board. The design of the circuitry makes use of a high-speed micro-controller, the 8X3ØØ, newly developed NMOS support devices, Schottky and low power Schottky devices. All I/O connections are made using standard ribbon cable connectors. Standard pin-out configurations for disk interface connectors permit direct pin-for-pin connections to the drives. All host to disk data transfers are buffered by onboard RAM to achieve totally asynchronous transfers to and from the disk by the host.

The disk controller is built around five basic sections:

Processor Functions

All functions of the controller are ultimately disciplined by the onboard processor. Due to the high data rates associated with hard disk drives, a processor capable of extremely fast execution speed is required for processing of data and controlling machine functions within the circuitry. The processor used is the 8X3ØØ, a bipolar micro-controller particularly well-suited for handling data efficiently at high rates.

The 8X3ØØ operates at a basic clock rate of 8MHz and performs all operations within two clock cycles giving it a speed of 4 MIPS (Million Instructions Per Second) or one instruction executed every 25Ø nanoseconds. The architecture of the processor is different from most popular microprocessors in that no common data or address bus is provided to be shared by RAM, ROM, or peripheral devices.

Instructions are fetched from ROM via a dedicated instruction address and data bus. The Instruction Address bus (IAØ - IA12) is capable of directly accessing 8K words of program storage, however, the controller uses only the first ten address lines, IAØ through IA9, limiting onboard program storage to 1K words.

Program information is input to the 8X3ØØ on the Instruction Bus (IØ-I15). This Bus is dedicated solely to receiving instructions from the ROMS, U34 and U41.

Fast I/O Select

An extension byte has been added onto the instruction data memory to provide port access decoding on an instruction-by-instruction basis. This "Fast I/O Select" byte is not processed by the 8X3ØØ, but it is decoded by auxiliary hardware (U39, U4Ø, U44 and U45) to provide eight read strobes and eight write strobes which route data to the various devices distributed along the interface vector bus.

The Fast I/O byte is latched into a 6-bit latch (U39) trailing edge of MCLK to ensure that the data remains stable during the entire instruction. This data selects a read strobe and eight write strobes which route data to the various devices distributed along the interface vector bus.

The Fast I/O byte is latched into a 6-bit latch (U39) trailing edge of MCLK to ensure that the data remains stable during the entire instructions. This data selects a read strobe and a write strobe through two 1-of-8 decoders (U44 and U45) which are alternately enabled by the WC* control strobe produced by the 8X3ØØ. The read strobe decoder (U44) is always disqualified at the end of instructions by MCLK' (MCLK prime), a delayed copy of MCLK, to provide edges on read strobes during sequential read operations from various ports. This delay compensates for timing races through the Fast I/O latch (U39) and the control signals.

Because each decoder has a unique input, it is possible to select any read port with any write port during each instruction. Data is transferred between the processor and its ports on a separate 8-bit bus called the I/O bus. This bus is active low. It must be noted that this bus is in no way related to the instruction data bus and should be thought of as simply an 8-bit bidirectional I/O bus of the 8X3ØØ. In fact, it has been renamed as IØØ - IØ7 to reflect this distinction.

Internal Bus Control

Several bus control signals are produced by the 8X3ØØ to identify and strobe the data on the I/O bus. Write Control

(WC) is a signal which determines the direction of the data to and from peripherals. When WC is false (during the first half cycle), data is being input to the 8X3ØØ from the I/O bus. When WC is true (during the second half cycle, data is being output to the I/O bus from the 8X3ØØ. Select Control (SC) becomes active during the second half cycle instead of WC if the I/O bus contains an 8-bit I/O address. the WC and SC signals are combined by a NOR gate (U33) to initiate all accesses from the 8X3ØØ to any output port within one instruction instead of the normal 5-bit immediate moves provided for by the instruction set.

All instruction fetches occur late in the second cycle of the preceding instruction. This time is marked by the generation of a 65 ns (nominal) active high pulse called MCLK which occurs every instruction. MCLK is used to latch data prior to being input on the I/O bus to ensure stability during reads. MCLK is also used to disqualify read strobes which would otherwise remain true into the second clock cycle of any instruction which does not write to a port.

There are two more bus control signals produced by the 8X3ØØ, Left Bank select (LB*) and Right Bank select (RB*). However, due to the implementation of the Fast I/O Select logic, only RB*, which is used as the chief enable signal for U17 and U18, is needed.

Reset Circuit

The 8X3ØØ is held reset for approximately 4Ø milliseconds after initial power-on. This is accomplished by an RC network (R42 and C52). After this power-up sequence, there are two ways to reset the processor, both of which are controlled by the host computer.

One method of resetting the processor is by resetting of the host (i.e., reset switch) which drives the signal HDMR* low. The other method of resetting the processor is by software control. This is accomplished by setting bit D4 of port C1 HEX. This latches the signal (SFTRESET) which in turn triggers a one-shot U76 to drive RESET* low. The one-shot duration is set for approximately 1ØØ micro second pulse width. RESET* is used to clear the drive control latches U62 and U52 and the host interface WAIT* (U43).

Processor Power Supply

Power is supplied to the 8X3ØØ from the +5 volt (Vcc) power bus. Due to the internal operation of the 8X3ØØ, an on-chip voltage reference is provided to produce bias to an external pass transistor (Q2) which drops Vcc to the 8X3ØØ to approximately +3 volts. All signals into and out of the 8X3ØØ are internally level shifted to be TTL compatible.

Read and Write Ports

Throughout the circuit, output ports are formed by "D" type latches using write strobes (WRØ -WR7) to latch data into the ports. Reading of ports is universally accomplished by using read strobes (RDØ, RD2, RD4 - RD6) that enable selected tri-state output devices on the I/O bus. Additionally, two read strobes are used to clock the host DRQ* and INTRQ* latches (U5) and one read strobe is left unused as a "dummy" port for glitch-free operation of the Fast I/O port decoders.

Read/Write Memory

Since the 8X3ØØ does not permit data to be saved or retrieved from dedicated program storage, RAM must be installed on the I/O bus. RAM must be accessed just like other port accesses via the I/O bus by I/O instructions. To provide for addressing the RAM, three latch/counters (U26, U27, U28) are connected to the I/O bus to receive and store addresses required to access the RAM (U17,U18).

RAM Addressing

The RAM address bus (RAØ - RA9) uniquely addresses one of 1Ø24 memory locations. As each counter chip reaches a count of Ø, it will set a borrow condition to the next higher counter which will be decremented at the end of the next access to RAM. When all bits of the address have been reset, the ROVF* bit on the last counter (U26) will be reset, providing overflow status which can be read by the processor on (U26). By setting various beginning address values, ROVF* can be used to mark the end of any RAM access loop from 1 to 1Ø24 bytes in length. The controller board uses this function to set sector buffer lengths of 128, 256, or 512 bytes.

Sector Buffering

All data read from or written to the disk is passed through the RAM to provide buffering required for asynchronous data transfer between the host and disk. The counters are post-decremented, which means that the effective addresses are stable to the RAM by at least the instruction prior to the actual access. This pre-selection feature effectively reduces RAM access time to the output enable and propagation time of the RAM for read operations. This feature also reduces the width of the minimum WR* strobe pulse for write operations.

RAM Accessing

RAM access is initiated by RCS* which is the logical OR (by U59) of RDO* and WRO* which are generated by the Fast I/O decoders (U44 and U45). Data to be read from RAM will be placed on the I/O bus whenever RCS* is low and WC* is high. Data is written into a selected RAM cell on the trailing edge of WC* if RCS* is low. During writes, both WC* and RCS* will be low for at least 12Ø nanoseconds so that data setup time requirements are met.

Scratchpad Operations

Because the RAM address counters can be pre-set, direct reads and writes to a specific address are possible. This function is used for scratchpad storage during program execution. This mode of RAM access requires two or three instruction cycles for each random access to the RAM as opposed to one for sequential access using the post-decrement feature.

MAC Control Port

Basic control of the various functional sections of the controller is accomplished by a dedicated 6-bit control port called MAC CNTRL (U29). MAC CNTRL enables CRC generation (CRCIZ*), functions of the WAIT control circuitry (WAEN*), gating of read or write functions (WRITE*), control of CRC check word output (1BLA*) One Byte Look Ahead, and AM detection (SRCH). MAC CNTRL output states are latched into the port by a write strobe (WR7). Additionally, any time MAC CNTRL is loaded with a new byte, the lower two data bits (IØØ and IØI) are strobed into the upper two address counter/latch bits (RA8 and RA9). All remaining ports are distributed among the basic functional sections of the controller and will be described in detail within the discussion of those functions.

Serial Data Separation

The controller board contains circuitry which processes incoming MFM data from the drive by a method called data separation. Here, some background information may be helpful:

> In order to provide maximum data recording density and therefore maximum storage efficiency, data is recorded on the disk using a Modified Frequency Modulation (MFM) technique. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. This reduces the total number of bits required to record a given amount of information on the disk. This results in an effective doubling of the amount of the data capacity, hence the term "double density."

Because clock bits are not recorded with every data bit cell, circuitry that can remain in sync with data during the absence of clock bits is required. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bits when they are present. This is accomplished by using a phase-locked oscillator employing an error amplifier/filter to sync onto and hold a specific phase relationship at the data and clock bits in the data stream. The synthesized clock called RCLK can then be used to separate data bits from clock bits and to shift the resultant serial data into registers for parallelization into bytes.

Incoming Data Selection

Serial data is input from up to four radially connected drives via a quad RS-422 differential receiver (U54). The receiver converts differential input data to TTL levels for use by the controller. The data from the selected drive is then routed to gate (U53). At this point, data and clocks are still combined and appear as 5Ø nanoseconds (nominal) active high pulses spaced at intervals of one, one and a half, or two times the RCLK period. This data is presented to the input of another AND/OR/INVERT gate (U4) which will gate either MFM data or a reference clock into the first stage of the VCO error amplifier circuitry.

Reference Clock

The reference clock is derived from the write clock crystal oscillator (Q1, U1Ø, and associated circuitry). This oscillator uses a fundamental cut crystal to oscillate at four times the RCLK frequency. The 4X output is then divided by U1Ø to produce both a 2X clock (2XDR*), which is used as a reference, and a 1X clock (WCLK) which is used to produce

MFM write data for the disk. The crystal (Y1) frequency is 20.000 MHz for compatible drives.

Clock Gating

The gating of the reference and MFM data into the data separator is dependent upon the condition of the Read Gate signal (RGATE) and the spacing of the data on the serial stream after RGATE is brought true. Due to the techniques which are employed to separate data from clocks, it is necessary to run the VCO at a rate twice the data clock (RCLK) rate. The VCO is therefore set to an open-loop frequency of 2 times RCLK. Any variations in this rate due to variations in disk rotational speed must be compensated for by the VCO, but instantaneous shifts in data due to the effects of adjacent bit cells on the disk and minor noise must be ignored. Also, the response of the VCO must be adjusted to effectively ride over missing clock bits which occur as a result of MFM recoding technique. The resultant compromise between response and reject requirements of the VCO cause the VCO to have a tendency to become locked onto harmonics of the data rate rather easily. This is likely to occur if the VCO is connected to a data stream over a field of data which has data bits spaced at one and a half or two times the actual RCLK time intervals.

To provide protection against this undesirable condition, the VCO is always held locked onto a stable clock running at two times the RCLK frequency whenever the controller is not actually reading data. Furthermore, great care is taken to switch in read data to the VCO error detector only when it is known that the data stream frequency is equal to the RCLK frequency. This can occur only when the data is a solid stream of all ones or all zeros.

High Frequency Detector

The switching function is initiated immediately after RGATE goes true and will only switch read data into the VCO after 16 consecutive ones or zeros (high frequency) are detected by a one-shot (U1) and counter (U2) connected directly to the raw MFM data. The one-shot is adjusted for a pulse width of one and one-fourth times the RCLK period. This is 25Ø nanoseconds, +/- 1Ø ns. These adjustments of the DRUN one-shot (U1) provide tolerances of up to one-fourth the RCLK period in jitter on the MFM data bits while still being able to distinguish MFM zeros or ones from other data patterns.
Each clock or data bit on the serial stream triggers the one-shot. If the time between successive triggers is less than the one-shot time constant, the one-shot remains retriggered. As the one-shot is triggered by data stream bits, so is the up/down counter (U2) whose count mode is controlled by the state of the one-shot outputs. While the one-shot is being retriggered, the counter counts up. When any data bit fails to reach the one-shot before its time constant is over, the one-shot resets and in turn clears the counter. Only when 16 successive retriggers occur, can the counter reach its terminal count. At this time, the counter overflow goes true and sets the DRUN* latch output (U3, pin 6) low which switches read data in and reference clock out. An AND-OR-INVERT gate (U4) performs the switching. DRUN* is read through (U74) by the 8X3ØØ to determine the condition of the MFM data stream.

VCO

The Hard Disk controller uses a single chip VCO (U32) which simplifies circuitry and adjustments. The operating point of the VCO is initially set by adjusting the variable capacitor (C33) for a 1Ø MHZ output at TP9 and the frequency control voltage input (TP8) to 2.5 V +/- .5 V. It should be noted here that both of these adjustments are done using the same trim cap (C33).

The output of the error amplifier and filter is fed to the VCO and represents how far the VCO frequency is from that of the incoming signal. The error signal, which is proportional to the difference, allows the VCO to shift from center frequency and become the same as the frequency of the frequency of the input signal. When the loop is in lock, the difference frequency component will be DC and is passed by the low pass filter.

Frequency control is actually a matter of frequency range. The difference component may fall outside of the band edge of the low-pass filter and be removed along with the sum frequency component. If this is the case, then no information is transmitted around the loop and the VCO remains at its initial free running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the filter. Now part of this difference component is passed which tends to drive the VCO to the frequency of the difference component more and allows more of it to be passed through the filter. This is a positive feedback, which causes the VCO to snap into "lock" with the input signal.

The term "capture range" can be described as the frequency range centered about the VCO free running frequency over which the loop can acquire lock with the incoming data signal.

The free running frequency of the VCO is always twice that of the RCLK rate. In fact, RCLK is produced by the VCO through a divide-by-two counter (U14).

Power for the VCO's internal oscillator as well as for the error amplification filter is supplied from a 78MO5 +5 volt regulator. This insures good noise separation for these stages from the power supply.

Error Amplifier

Control of the VCO is accomplished by the error amplifier, filter, and Data Separator chip. The error amplifier is a balanced current mirror whose output sources or sinks current to the filter stage. Whenever the VCO is running too slow, the error amplifier receives pulses from data bits before pulses from the VCO clock. This causes the error amplifier to produce pump-up pulses to the filter. The filter integrates these UP pulses and raises the overall voltage of the voltage control input (TP8) to the VCO. When the VCO is running too fast, the error amplifier produces pump-down pulses to the filter. There will always be some error present because without pulses of UP and DN the filter would float causing the VCO to drift off center frequency.

Phase Detector

The circuitry which feeds the error amplifier is called the phase detector. This consists of several "D" latches (U2Ø, U21) and a delay line (U31). The function of this circuit is to provide time windows during which the leading edges of the incoming MFM data can be compared to the leading edges of the VCO clock. These windows are approximately 5Ø nanoseconds in length and are initiated by the leading edge of any data bit as it enters the detector. The windows are terminated by the same data bit, edge delayed by a net of 5Ø nanoseconds (6Ø nanoseconds in the delay line minus approximately 1Ø nanoseconds in propagation delays.) When both the delayed data bit and the nearest VCO clock edge arrive at the detector, the detector is reset until the next data bit arrives on the MFM data stream. The delayed data bit sets its half of the detector latches to produce the VP pulses. The VCO clock edge sets its half of the detector to produce the DN pulse.

Window Extension

Once the VCO has been locked onto the phase of the incoming data, the actual separation of data and clocks can occur. This is accomplished by using a technique called window extension. This technique causes data bits to first have their leading edges shifted into the center of the RCLK half cycles then to have them latched or extended until the next rising edge of the RCLK. The shift is accomplished by tapping the data of the Sample on Phase Detector delay line at the 6Ø nanosecond tap, and inverting the VCO clock to the RCLK divider (U14). The delayed data clocks a pair of latches (U12 and U13). The "data" latch has its "D" input and CLEAR connected to RCLK* and the "clock" latch has its "D" input and CLEAR connected to RCLK*.

If an MFM data bit enters the latches while RCLK is high, it will be extended as a data bit. If RCLK* is high, it will be extended as a clock bit. Due to this extension technique, bits can jitter approximately one-fourth the RCLK period without being lost. The output of each latch is then further extended by being fed directly into the second half of the latches and clocked on alternate edges of RCLK. The final outputs of the data extension/separation stage are two separate signals; one signal consists solely of NRZ (non-return to zero) data and the other of NRZ (non-return to zero) clocks. The NRZ data and clocks are finally in a form suitable for processing by subsequent circuitry on the Controller board.

Clock Detection

Due to the nature of MFM data encoding, it is impossible to know exactly if MFM bits are data or clocks. This ambiguity results in having to create circuitry to assume that bits on RCLK* are actually data bits until the VCO is locked on and a unique data/clock pattern is detected. This is accomplished by holding the VCO to RCLK divider (U14) reset until it is fairly certain that bits on the data stream are actually clocks belonging to a field of zero data.

Once this assessment has been made, the processor releases the AM (Address Mark) detector (U11) by raising the SRCH signal. This signal releases a latch (U2Ø) which will remove DHOLD from the RCLK divider (U14) on the next rising edge of a MFM data bit so that CLOCKS will be on the RCLK* phase and DATA will be on the RCLK phase. The processor makes its assessment of the state of the data stream solely on the occurrence of a significant run of zeros which is detected by the one-shot (U1) in the DRUN circuit. Once released, the phase of RCLK vs. data and clocks will remain stable throughout the read of an ID field or data field. Whenever SRCH is dropped, the VCO to RCLK divider is once again reset and no RCLKS are produced.

Data Conversion and Checking

MFM data which has been separated to form NRZ data and clocks is processed through specialized circuitry to prepare it for parallel processing by the 8X3ØØ. This processing consists of three functional circuits.

1. AM detection (U11)
2. Serial-to-Parallel conversion (U9)
3. CRC checking circuit (U6)

Each function will be discussed separately but bear in mind that many interdependencies exist.

AM Detection

As previously stated, it is impossible to know whether serial data bits are actually data or clock bits by just looking at the data stream. Furthermore, it is equally impossible to determine byte boundaries. The problem is solved by a uniquely recorded data/clock pattern called an Address Mark (AM). The AM consists of a data pattern of HEX 'Al' with a missing clock pattern of HEX 'ØA'. Normally a data byte of of HEX 'Al' requires a clocking pattern of HEX 'ØE'. In fact, due to the rules of MFM data encoding, an alternating clock pattern such as HEX 'A' or HEX '5' cannot exist legally.

The AM is used to uniquely identify the start of a field of information (data or ID field) within each sector. A long run of zero data always precedes each AM on the disk. Zeros have a clock bit for every RCLK. When attempting to read information from the disk, the Controller first acquires phase lock over a field of zeros. When this acquisition is achieved, the processor releases the AM detector (Ull) by raising the Search control line (SRCH) on the MAC CNTRL port (U29).

D e to the circuitry associated with the VCO to RCLK divider, the RDAT* output of the data separator (Ul3 - 8) will be high and the CLKS* output (Ul2 - 8) will be low. RCLK* will be the shifting clock for RDAT* and RCLK will be the shifting clock for CLKS*. These four signals are routed into the AM detector. Inside the AM detector, RDAT* is shifted into an 8-bit synchronous serial shift register and clocked on the falling edge of RCLK*. CLKS* is shifted into a similar shift register on the falling edge of RCLK. The output stage of the RDAT* register is dumped into an 'Al' comparator and the output stage of the CLKS* register is dumped into a 'ØA' comparator. AM detection occurs when both detectors are true, thereby setting the AMDET* latch. At the instant AM occurs, the exact relationship between data and clocks is known. It is also known that data is being clocked by RCLK* so CLKS* can actually be discarded; their purpose was in detecting AM. The AMDET* signal is used as a synchronization signal to start subsequent conversion circuitry. The AMDET* signal remains true until the processor again de-asserts the Search control line.

Serial to Parallel Conversion

After an AM (Address Mark) has been detected, the serial-to-parallel convertor (U9) takes over. NRZ data and RCLK are used to shift data bits into an 8-bit serial-to-parallel shift register. As each bit is shifted, a divide-by-8 counter circuit is incremented. After every eighth bit of data is shifted, the counter produces an overflow pulse marking byte boundaries in the serial data stream. The overflow bit from the counter resets the counter, clocks the data from the shift register into an 8-bit parallel latch, and sets a tri-state flag register called BDONE. The flag can be read by the processor to see if any converted data is ready to be read from the latches.

When the processor sees BDONE in the true state, it services the device by gating data onto the I/O bus using read strobe 4 (RD4*) in conjunction with a tri-state buffer (U8). The act of reading the latches also clears off the pending BDONE flag. As successive bytes are processed, the BDONE is serviced by the processor as data becomes available.

Outputs from the serial-to-parallel device also include SHFTCLK* and DOUT. SHFTCLK* is actually RCLK* propagated through the device. DOUT is the Q output of the last stage of the shift register string. DOUT and SHFTCLK* are routed to the CRC generator checker device and also are tri-stated along with BDONE. These signals are active only when WRITE* is high which indicates a read mode of operation.

CRC Checking Circuit

Data recorded on magnetic media is prone to several types of errors which could render data unusable if some form of error detection were not employed. Therefore, a Cyclic Redundancy Check (CRC) is performed on all data transfers from the disk. The CRC is an error detection code consisting of 16 additional bits which are appended to every ID field and data field on the disk. These bits are produced by dividing the data stream serially with a large polynomial. This division produces a unique 16-bit value for any information passed through the CRC generator.

As data is being read from the disk, the CRC generator (U6) re-computes the original CRC bits. The value in the CRC generator must always be zero after the last two bytes (which contain the orginal recorded CRC) are read. When this happens, the data was correctly read and the controller will not flag an error. If, however, the CRC generator is not zeroed after it has checked all bytes of the recorded data, the controller will flag the data as erroneous and enter into a re-try condition. If the controller cannot get correct data after attempting to read it 16 times, the read will be aborted and the host informed that the data in the buffer is questionable.

The Controller board uses the same device to generate and check CRC's for data being written to or read from the disk. The polynomial used is:

$$X^{16} + X^{12} + X^{5} + 1$$ (commonly called the CRC-CCITT polynomial)

The processor polls the condition of the DRUN circuitry during read operations. When DRUN is true, it begins to search for an Address Mark. Once the AM is located, the processor will start to read parallel data which has been converted from NRZ data by the serial-to-parallel device. The processor will terminate this activity when it has received the information it is looking for or if an error is detected.

While the processor is reading the parallel data, the CRC generator is reconstructing the CRC check value. The CRC generator is initialized by the processor setting CRCIZ* low

for at least 25Ø nanoseconds during the search for the AM. CRCIZ* is originated on the MAC CNTRL port (U29). Upon receiving the CRCIZ* signal, the CRC generator/checker will preset all 16 of its internal polynomial division shift registers to logic ones and arm an internal latch which will enable the checking function on the leading edge of the first non-zero data to enter the device. It should be remembered that prior to an AM there is always a field of zeros (all data bits low) so the first non-zero data bit into the device will always be the most significant bit of the AM (HEX A1).

The CRC device, when enabled by the first non-zero data bit, will shift succeeding data bits into a feedback shift register string with Exclusive OR gates tied to the feedback nodes on the first, fifth, twelfth, and sixteenth registers. As each RCLK occurs, the registers will divide the incoming data and a unique pattern of ones and zeros will appear across the registers.

When the last bit of an ID or data field is processed, the pattern in the registers should be equivalent to the 16 bits appended to the fields during original recording. The appended bits are also entered into the CRC device. If all of the bits in the appended field are identical to the bits in the registers, then the Exclusive-or-Gates in the register string will have flipped all of the ones to zeros and the CRC will have been satisfied.

The output of each register stage is tied to a 16-bit comparator which goes true when all of its inputs are zeros. The output of the comparator is retimed to remove any decoding slivers and is output as CRCOK. The processor can read CRCOK through U61 to see if a CRC error has occurred.

After the CRC bits are processed, the data stream will contain at least one more byte of zeros. It is the nature of the CRC polynomial that if no bits are set to ones in the registers and if a constant input of zeros is shifted into the registers, no bits will be flipped. This provides a convenient latching function for the CRCOK flag which will remain true for at least one byte after the last CRC check byte, giving the processor time to read the flag.

The data, clock, and BDONE are supplied to the CRC device on a 3-bit mini bus. During read operations, the serial-to-parallel device (U9) will be sourcing these lines since the WRITE control line from MAC CNTRL (U29) is low and this enables tri-state drivers on these lines. The Parallel-to-Serial device (U7) will have its tri-state drivers disabled.

Serial Data Generation

The Controller records data on the disk in MFM format. In order to produce the proper data format, the Controller uses several specialized devices to process the parallel data supplied by the host into a serial MFM data stream. The data supplied by the host is temporarily stored in the buffer RAM until the correct sector is located for the data to be written.

The process of writing is essentially the opposite of reading except that the data separator circuitry is not required and the generation of the MFM data stream is produced by synchronous clocking techniques.

The functional sections of the serial data generation section are listed below:

1. Parallel-to-Serial conversion (U7)
2. CRC generation (U6)
3. MFM and precompensation (U5)

Parallel to Serial Conversion

Parallel data is converted into a serial NRZ data stream by the parallel-to-serial device (U7). The processor enables this conversion by lowering the WRITE* signal on MAC CNTRL (U29). WRITE* causes the tri-state buffers present on the parallel-to-serial device to become active, supplying the CRC device with data, clocks, and BDONE strobes.

The processor presents parallel data on the I/O bus along with the WR4* write strobe which latches the data into the parallel port on the BDONE. Inside the parallel-to-serial device, the parallel latches are loaded into a serial shift register on every eighth WCLK transition. As the data is transferred to the shift registers, the BDONE status flag is set. The processor reads this flag through U61 to determine when to write the next parallel byte to the device. The timing of the parallel accesses is at a rate one-eighth that the bit rate of the NRZ data stream.

The output of the last register in the shift string is brought out of the device as a NRZ serial data stream. The shifting clock is also brought out as SHFTCLK to be used as the clock for the CRC device.

Whenever it is desired to write a repetitive string of identical data bytes, the processor can simply ignore the BDONE flag and permit the device to reload the data from its latches over and over again for as long as required to generate the field. This feature of the device is used in writing certain fields used in formatting.

CRC Generation

The CRC generator/checker (U6) is used to generate the CRC bits and to append them to the end of the data being written to the disk. This is the complementary function to that performed during reads. The operation of the polynomial generator is identical to read operations except that at the end of the data field, the processor sets a signal which causes the device to output the computed CRC after the data instead of reading the CRC and checking it.

The initial state of the shift registers within the device is forced to all ones by the processor pulsing CRCIZ* for approximately 25Ø nanoseconds while the parallel-to-serial device is outputting all zeros on the NRZ data line. At that time, a latch is set which holds the registers at ones until the first non-zero bit enters the device. The first non-zero bit will be the MSB of the AM (HEX A1) of the data field to be written. When the processor decides that enough zeros have been written to satisfy the sync field requirements, it will store a HEX A1 in the parallel-to-serial device. At the proper time (in sync with BDONE) the parallel-to-serial device will begin to send the MSB of the AM to the CRC device. This will start the CRC polynomial generator and the CRC will be computed.

As the processor writes the last byte of data to the parallel-to-serial device, it will drop the 1BLA* (1 Byte Look Ahead) signal on MAC CNTRL port (U29). This signal will cause the CRC generator (U6) to begin dumping the computed CRC onto the NRZ data stream at the conclusion of the last data byte (synchronized with the BDONE signal). In this fashion, the device is able to append the proper CRC information to the end of a field of data. 1BLA* is maintained at a low state for the duration of the unloading process which lasts for 16 bit times.

During the unloading process, the CRC registers back-fill with zeros. This feature is handy because by leaving 1BLA* low; for additional time, zeros will always be written after the CRC which is a requirement for the proper operation of

the CRC device during read operations. The NRZ data with CRC appended is then sent to the MFM generator device (U5).

MFM Generation

The conversion from NRZ write data to MFM write data takes place in the MFM/Precompensation device (U5). This device accepts NRZ data and a complimentary WCLK and produces MFM data and clocks by sending the data through circuitry which decides when and where to write clocks on the data stream under the MFM encoding rules. The proper encoding of the data into MFM requires the device to apply three rules to the data.

1. If the current data cell contains a data bit, no clock bit will be generated.

2. If the previous data cell contained a data bit, no clock bit will be generated.

3. If the previous data cell and the present data cell are vacant, a clock bit will be produced in the current clock cell.

The terms "data cell" and "clock cell" are defined by the state of WCLK. While WCLK is low, it is a data cell and while high, it is a clock cell. It can be seen then that both clock and data cells are one-half the period of WCLK or 100 nanoseconds. Also note that by the rules started above, a clock and data bit can never occur within the same WCLK period and legal spacings for bits can be one, one and a half, or two times the WCLK period only. The rules are implemented within the device by shift registers that hold the next two, last, and present data bits and combinational logic. The state of WCLK is considered and the appropriate bit cells are filled and combined on the MFMW output line of the device. This line is subject to decoding slivers, so it is run through a re-timing latch (U16) to clean it up.

Write Precompensation

The MFM data stream is now totally compatible with the recording rules and may be sent to suitable line drivers for transmission to the drive except for one modification. Due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem in magnetic recording known as dynamic bit shift.

Dynamic bit shift occurs as the result of one bit on the disk (a flux reversal) influencing an adjacent bit. The effect is to shift the leading edge of both bits closer together or further apart than recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error. In any event, there is a method called write precompensation which can be applied to reduce the effect of this shift on the data.

Write Precompensation is a way of predicting which direction a particular bit will be shifted and intentionally writing that bit out of position in the opposite direction to the expected shift. This is done by examining the next two data bits, the last bits, and the present bits to be written and producing three signals depending on what these bits are. The three signals are EARLY, LATE, and NOM. They are used in conjunction with a delay line to cause the leading edge of a data/clock bit to be written early, late, or on time. As with MFMW, (MFMW Write Data) these signals are subject to decoding slivers and must be retimed by U16.

The processor can enable or disable the generation of these signals by controlling the RWC (Reduce Write Current) line from U52. When RWC is high, precompensation is in effect. When RWC is low, no precompensation is generated and the NOM output of the device is held true.

The delay line, U31, actually performs the precompensation with the help of an AND-OR-INVERT gate (U37). The MFMW pulses are applied to the input of the delay line and, depending on which of the three precompensation signals is present, the U37 selects a different tap on the delay line. Nominal data is actually tapped from the second tap, early data from the first, and late data from the third. From U37, the MFMW data is sent to the input of a quad driver (U35 or U36) where it is converted to a differential form and then sent to the disk drive. The AND-OR-INVERT gate (U37) has one other function. If the controller is not writing, the WGI (Write Gate Internal) signal will be low. This is inverted by U19 and applied to the fourth section of U37. This resulting high input effectively inhibits the gate from accepting MFMW data.

Host Interface

The interface bus to the controller is pin-for-pin compatible with the standard I/O port. This includes an 8-bit bidirectional data bus (U7Ø) and 8 address lines (U71). For systems using interrupts and/or DMA, the controller also provides Interrupt Request (HDBINTRQ*) and Data Request (HDBDRQ*).

Accessing the controller is like other I/O devices. Address decoding is done on the controller board by U69. This decode can be jumpered to recognize four different address ranges. Standard setting is jumpered from 17 to 19, which utilizes port locations CØ to CF HEX. Further decoding to allow access of specific ports is done by U66, U67, and U68. Data bus direction is determined by U56, using standard bus as well as decoded signals.

Wait Enable

The generation of the WAIT* signal is controlled by a bit in the MAC latch (U29) called Wait Enable (WAEN*). If the controller is ready to accept random access to its task file, WAEN* will be asserted. After WAEN* is clocked through a latch (U43) to insure WAEN* is not asserted during a bus access in progress, DCRCS* (BIC or BOC in some applications) causes WAIT* to be asserted to the bus.

The WAIT* line is released on the trailing edge of any Read or Write Strobe to the communications latch, U6Ø. This release is caused by the logical OR of RDG* and WRG* on U38 which presets the wait latch, U43, to a non-wait request condition.

INTERRUPTS AND DRQ'S

The controller produces INTRQ* to signal the end of all disk operations and DRQ's to signal data ready to DMA controllers. INTRQ* and DRQ* originate on the MFM generator (U5) as an auxiliary function of that chip. The INTRQ* signal is set using INTCLK and the DRQ signal is set using DRQCLK, both of which are produced by U44. Interrupts are cleared by CSAC* (A 2ØØ nanosecond version of the CSAC signal) and AØ, Al whenever the host reads the status register, issues a command or accesses the sector number register. Data requests (DRQ's) are cleared when the host accesses the data or cylinder low registers DRQ's will be reissued for each byte to be transferred. During power on or Master REsets (MR*), INTRQ* is set and DRQ is reset.

Appendices 12/15 Meg

Appendices which describe the hard disk drive are included with the 12/15 Meg Hard Disk Service/Technical Reference Manual. The 12 Meg drive uses the Tandon TM6Ø2S, TM6Ø3S AND TM6Ø3SE Disk Drive assembly (Tandon Publication 187275-ØØ4 (REV C). The 15 Meg drive uses the Tandon TM5Ø3 Disk Drive assembly (Tandon Publication 179Ø45-ØØ1A [T5ØØ3 A 2-83]) All disk drive specifications, operating instructions, troubleshooting procedures, spare parts, circuit board schematics and assembly drawings for the unit are included.

Controller Board - WD1Ø1Ø Based

The WD1ØØØ-TB1 is a stand-alone Winchester Disk Controller board designed to interface up to four Winchester Disk drives to a TANDY-HDC or a compatible bus.

Communication to and from the host computers are made via 8-bit bi-directional data bus and appropriate control signals. All data to be written to or read from the disk, status information, and Macro commands are transferred via this 8-bit bus. An on board sector buffer allows data transfers to the host computer independent of the actual data transfer rate of the drive.

The WD1ØØØ-TB1 design is based upon propriety chips WD1Ø1Ø (Winchester disk controller) and WD11ØØ (Winchester disk controller support).

Features

- Built in Data Separator.
- Built in Write Precompensation Logic.
- Data rates up to 5 Mbits/sec.
- Control for up to four drives.
- Control for up to 8 R/W heads.
- 1Ø24 Cylinder Addressing Range.
- 256 Sector Addressing Range.
- CRC Generation/Verification on ID Fields.
- Automatic formatting.
- 128, 256, 512, 1Ø24 Bytes per Sector (user selectable).

Features cont.

- Unlimited sector interleave capability.
- Overlap seek capability.
- Implied seek on all commands.
- MFM encoding recording.
- Automatic retries on all errors.
- Programmable step pulse rates between 35 usec and 7.5 Msec.
- Automatic restore on all seek errors.
- Programmable disk parameters.
- Error reporting (Disk/Controller errors).

Specifications

Drive Specifications:

Encoding method	MFM
Cylinder per head	1Ø24
Sectors per track	Up to 256
Heads	8
Drive Selects	4
Step rates	35 u sec to 7.5 Ms
Data transfer rate	5.ØØØ Mbits/sec
Write precomp time	12-15 ns
Sectoring	Soft
Drive Capability	1Ø LS loads
Cable length (drive)	1Øft. (3M) max.

Environmental Specifications

The controller module is designed to withstand the following environmental conditions.

A. Temperature:

Operating Range	Ø to 5Ø°C

B. Relative Humidity:

Operating Range	2Ø% to 8Ø%

Note: The range of relative humidity is established on the basis that no condensation is permitted.

C. Reliability:

Mean time between failure (MTBF) is greater than 1Ø,ØØØ hours.

Board Outline

Figure 4. shows the outline for the WD1ØØØ-TB1 board. All connectors are specified in Tables 1 through 5.

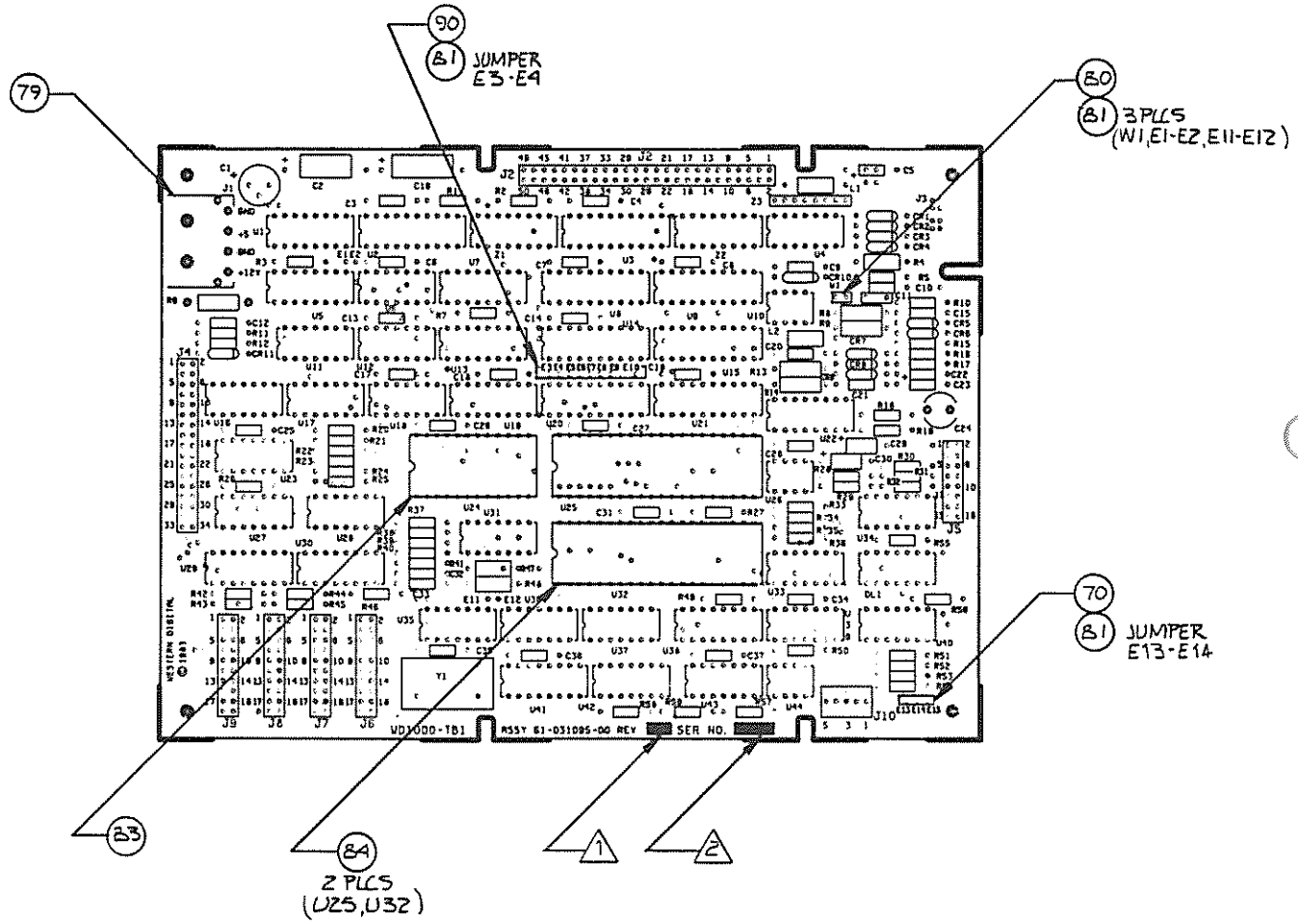


TABLE 1

CONNECTOR J1		CONNECTOR J2		CONNECTOR J3		CONNECTOR J4	
PIN #	SIGNAL	PIN#	SIGNAL	PIN#	SIGNAL	PIN#	SIGNAL
1	DRSEL	1	DRSEL	1	DRSEL	1	DRSEL
2	GND	2	GND	2	GND	2	GND
3		3		3		3	
4	GND	4	GND	4	GND	4	GND
5	WPD1*	5	WPD2*	5	WPD3*	5	WPD4*
6	GND	6	GND	6	GND	6	GND
7		7	PUP(12V)	7	PUP(12V)	7	PUP(12V)
8	GND	8	GND	8	GND	8	GND
9		9		9		9	
1Ø		1Ø		1Ø		1Ø	
11	GND	11	GND	11	GND	11	GND
12	GND	12	GND	12	GND	12	GND
13	+MFMD	13	+MFMD	13	+MFMD	13	+MFMD
14	-MFMD	14	-MFMD	14	-MFMD	14	-MFMD
15	GND	15	GND	15	GND	15	GND
16	GND	16	GND	16	GND	16	GND
17	IN-	17	IN-	17	IN-	17	IN-
18	IN+	18	IN+	18	IN+	18	IN+
19	GND	19	GND	19	GND	19	GND
2Ø	GND	2Ø	GND	2Ø	GND	2Ø	GND

(DATA CABLE)

TABLE 2

CONNECTOR J5

PIN NUMBER	SIGNAL
1	GND
2	RWC*
3	GND
4	HSEL2*
5	GND
6	WGI*
7	GND
8	SC
9	GND
1Ø	TRK*
11	GND (DRIVE CONTROL CABLE)
12	WF*
13	GND
14	HSELO*
15	GND
16	
17	GND
18	HSEL1*
19	GND
2Ø	INDEX*
21	GND
22	READY*
23	GND
24	STEP*
25	GND
26	DRS1*
27	GND
28	DRS2*
29	GND
3Ø	DRS3*
31	GND
32	DRS4*
33	GND
34	DIR IN
22	

TABLE 3

CONNECTOR J7 (TOP)				CONNECTOR J7(BOTTOM)			
PIN NO.			SIGNAL	PIN NO.			SIGNAL
30	1	(D0)	HDBD0		26		GND
	2		GND	35	27	(A5)	HDBA5
22	3	(D1)	HDBD1		28		GND
	4		GND	38	29	(A6)	HDBA6
32	5	(D2)	HDBD2		30		GND
	6		GND	36	31	(A7)	HDBA7
26	7	(D3)	HDBD3		32		GND
	8		GND	19	33	(IN*)	HDBRD*
18	9	(D4)	HDBD4		34		GND
	10		GND	12	35	(OUT*)	HDBWR*
24	11	(D5)	HDBD5		36		GND
	12		GND	2	37	(SYSRES*)	HDBMR*
14	13	(D6)	HDBD6		38		GND
	14		GND		39	(NC)	HDBINTRQ*
20	15	(D7)	HDBD7		40		GND
	16		GND	33	41	(WAIT*)	HDBWAIT*
25	17	(A0)	HDBA0		42		GND
	18		GND		43	(NC)	HDBSEL
27	19	(A1)	HDBA1		44		GND
	20		GND		45	(NC)	HDBDRQ*
40	21	(A2)	HDBA2		46		GND
	22		GND	14	47	(INTAK*)	HDBM1*
34	23	(A3)	HDBA3		48		GND
	24		GND		49		HDB IORQ*
31	25	(A4)	HDBA4		50		GND

Note: * Indicate Control Signals.

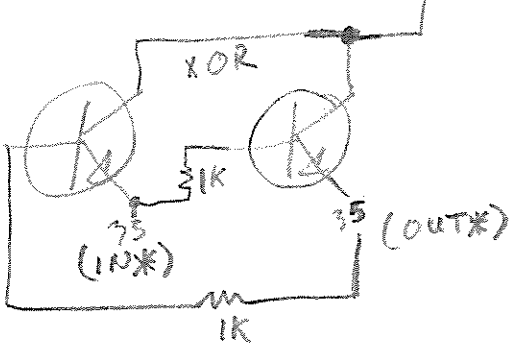


TABLE 4

POWER CONNECTOR

CONNECTOR J8

1	+12 VDC
2	GND
3	+5 VDC
4	GND

TABLE 5

ACTIVE LED CONNECTOR

CONNECTOR J9

1	Control 1
2	Control 2
3	GND
4	Driver
5	+5V

Note: This connector is implemented for the indicator LED.

Straps and Options:

All of the options and straps available on WD1ØØ1-TB1 are described in the following sections, however, some references are made to these options in other sections where their use is more fully described.

Please note that permanently installed options need not be changed for standard board practices.

The following list of straps are non-user options and are used solely for manufacturing test purposes.

W1	VCO Input
E11	Crystal Isolation

The following list of straps are user options.

E1 -E2	Software reset option
E13-E14	Write protect disable
E7 -E8	Select 5X
E9 -E1Ø	Select 6X
E5 -E6	Select 7X
E4 -E3	Select CX
E13-E14	

INPUT & OUTPUT PORTS

DEC 80 — 95
96 — 111
112 — 127
192 — 207

Related Documents:

Document Number	
TRS - 8Ø 5M HARD disk users manual	26-113Ø
TRS - 8Ø 12M Hard disk users manual	26-4152
WD1ØØØ-TB1 Test Specification	Preliminary
WD11ØØ-11 Product Specification	29ØØØØ25-ØØØ5
WD1Ø1Ø, Ø8 Data Sheet	-

Theory of Operations

Host Interface Signals

The Host Interface Connector (J7) consists of an eight bit bi-directional bus, eight bit address bus, and eight control lines.

The host interface pins and signals are illustrated in Table 1.

HDBDØ - HDBD7 NOTE 1:*

8-bit bi-directional data access lines. These lines are tri-stated by WD1ØØØ-TB1 board whenever the WD1Ø1Ø is utilizing the internal data bus. (BCS* is asserted). Otherwise the information on the data bus is driven onto the internal data bus of the WD1ØØØ-TB1. This is accomplished by leaving the HDSEL* signal at logical low level when the board is not selected.

HDBWR*

When Write Enable is active and the target register on WD1ØØØ-TB1 board is selected, the host may write data to the selected register.

HDBRD*

When Read Enable is active and the target register on WD1ØØØ-TB1 board is selected, the host may read data from the selected register

*NOTE 1

These signals are transmitted/received using an Octal bus transceivers that have the following characteristics;

IOL = 48 ma at .5V max.

IOH = 3 ma at 2.4V min.

HDBSEL*

This signal is asserted when the host initiates a read operation to the WD1ØØØ-TB1 board.

HDBDRQ*

The Data Request line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host.

HDBM1*

This signal identifies the instruction fetch cycle of the host. It is also asserted in conjunction with HDBIORQ* to indicate an interrupt acknowledge.

HDBINTRQ*

The interrupt request line is activated whenever a command has been completed, if so programmed by the host.

HDBMR*

Master reset signal initializes all internal logic on the WD1ØØØ-TB1 board. This line must be asserted for at least 5 micro seconds.

HDBIORQ*

This line identifies in I/O operation cycle of the host it is also used in conjunction with HDBMI* to indicate an interrupt acknowledge.

HDBA0- HDBA7

The eight address lines. These lines are decoded by the WD1ØØØ-TB1 to select one of the internal registers during Read/Write operations to these registers.

General Description

All interfacing is done through the Host Interface Connector (J7). All data transfers between the host and WD1ØØØ-TB1 board take place over an eight bit bi-directional bus consisting of eight data lines. (HDBDØ-HDBD7). The source and destination registers inside the WD1ØØØ-TB1 are selected by decoding eight address lines (HDBAØ-HDBA7). Data is passed between the interface board and the system bus via a 74LS645-1 transceiver. Address and control signals are taken off of the system bus and are buffered using 74LS244 receivers.

The primary interfacing to the system bus consists of misc. read and writes to and from a bank of registers used to hold parameter information pertaining to each command or initiation signals. The register values controlling the operations are mostly implemented inside the WD1Ø1Ø chip, however, two Read ports and a Write port are implemented externally.

There are four board select lines and they are decoded using HDBA7 - HDBA4 as follows:

A7	A6	A5	A4	A3	A2	A1	AØ	Board Select
Ø	Ø	Ø	Ø	X	X	X	X	None
Ø	Ø	Ø	1	X	X	X	X	None
Ø	Ø	1	Ø	X	X	X	X	None
Ø	Ø	1	1	X	X	X	X	None
Ø	1	Ø	Ø	X	X	X	X	None 5X
Ø	1	1	Ø	X	X	X	X	Port 6X
Ø	1	1	1	X	X	X	X	Port 7X
1	Ø	Ø	Ø	X	X	X	X	None
1	Ø	Ø	1	X	X	X	X	None
1	Ø	1	Ø	X	X	X	X	None
1	1	Ø	Ø	X	X	X	X	Port CX
1	1	Ø	1	X	X	X	X	None
1	1	1	Ø	X	X	X	X	None
1	1	1	1	X	X	X	X	None

- Port 5X will be selected if E7-E8 jumper is installed.
- Port 6X will be selected if E9-E1Ø jumper is installed.

- Port 7X will be selected if E5-E6 jumper is installed.
- Port CX will be selected if E4-E3 jumper is installed.

Within the addressing range associated with each board address. Two read ports and one write port are selected when the following conditions are present: The following table is generated for board address CX;

HDB RD*	HDB WR*	HDB M1*	HDB IORQ*	HDB A7-HDBAO	Port
Ø	1	1	Ø	CØ	Read Port Ø
Ø	1	1	Ø	C1	Read Port 1
1	Ø	1	Ø	C1	Write Port 1

All other combination of HDBRD*, JDWR*, HDBM1* and HDB IORQ* will not produce any read or writes for the C2 through C7 addressing range, however C8 through CF are used to address the task registers inside for the WD1Ø1Ø chip (see Programming (Task File) for more details) as shown.

HDB RD*	HDB WR*	HDB M1*	HDB IORQ*	HDBBA7-HDBAØ	Port
Ø	1	1	Ø	C8	Data
Ø	1	1	Ø	C9	Error Flag
Ø	1	1	Ø	CA	Sector Count
Ø	1	1	Ø	CB	Sector Number
Ø	1	1	Ø	CC	Cylinder Low
Ø	1	1	Ø	CD	Cylinder High

HDB RD*	HDB WR*	HDB M1*	HDB IORQ*	HDBA7 HDBAO	PORT
Ø	1	1	Ø	CE	SDH
Ø	1	1	Ø	CF	Status Register
1	Ø	1	Ø	C8	Data
1	Ø	1	Ø	C9	Write Precomp Cylinder
1	Ø	1	Ø	CA	Sector Count
1	Ø	1	Ø	CB	Sector Number
1	Ø	1	Ø	CC	Cylinder Low
1	Ø	1	Ø	CD	Cylinder High
1	Ø	1	1	CE	SDH
1	Ø	1	1	CF	Command Register

All other combinations of HDBRD*, HDBWR*, HDBM1*, HDBIorQ* and board address selects C2 through C7 will not produce any read or writes on WD1-TB1 board.

Prior to initiating an operation, the host must initialize the appropriate registers inside the WD1ØØ-TB1 board.

For details on programming the WD1Ø1Ø refer to section 4, however the external registers and their programming is described in the following tables and notes associated with each table.

Write Port 1 is loaded from the data bus when the Write Enable to this port is asserted. (WRDIRI*)

DATA LINES	WRITE PORT 1
HDBDO	"X"
HDBD1	"X"
HDBD2	"X"
HDBD3	DEVEN
HDBD4	SFTRST
HDBD5	"X"
HDBD6	"X"
HDBD7	"X"

Device Enable (DEVEN) must be initialized to "1" before the WD1ØØØ-TB1 responds to any commands.

Software reset (SFTRST) will cause a master reset to internal logic on the WD1ØØØ-TB1 board.

When a Read from Port Ø (RDDIRØ* is asserted) is initiated the following information will be driven onto the data bus.

READ PORT Ø	DATA LINES
INTRQ	HDBDØ
HWPL	HDBD1
"Ø"	HDBD2
"Ø"	HDBD3
WPD4	HDBD4
WPD3	HDBD5
WDPD2	HDBD6
WPD1	HDBD7

INTRQ:
Interrupt request line.

HWPL:
This signal indicates that at least one of the four disk drives is Write Protected.

WPD1 - WPD4

Write protect from Drive One through Drive Four. When a Read from Port 1 (RDDIR1* is asserted) is initiated the following information will be driven onto the data bus.

READ PORT 1	DATA LINES
"X"	HDBDØ
"X"	HDBD1
"X"	HDBD2
DEVEN	HDBD3
SFTRST	HDBD4
"X"	HDBD5
"X"	HDBD6
"X"	HDBD7

Reading from this port allows the host to verify the information loaded into the Write Port 1 register.

The WD1ØØØ-TB1 provides facilities (LED drive) to turn an LED on whenever the disk drive READY signal is asserted. This is accomplished through Connector J1Ø.

The WD1ØØØ-TB1 also provides a software reset mechanism that is activated by assertion of SFTRST signal. The width of this reset is programmed to be nominally at 1Ø us.

Programming

Task File:

The task file is a bank of registers used to hold parameter information pertaining to each command.

These registers and their addresses are:

A2	A1	A2	READ	WRITE
Ø	Ø	Ø	Data	Data
Ø	Ø	1	Error Flags	Write Precomp Cylinder
Ø	1	Ø	Sector Count	Sector Count
Ø	1	1	Sector Number	Sector Number
1	Ø	Ø	Cylinder Low	Cylinder Low
1	Ø	1	Cylinder High	Cylinder High
1	1	Ø	SDH	SDH
1	1	1	Status Register	Command Register

Error Flags:

This read only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	Ø
BB	CRC	-	ID	-	AC	TK	-

Bit 7 - Bad Block Detect

This bit is set when ID field has be encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 - CRC Data Field

This bit is set when a data field CRC error has occurred or the Data Address mark has not been found. The sector buffer may still be read but will contain errors.

Bit 5 - Reserved

Not used, forced to a zero.

Bit 4 - ID Not Found

This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occurred.

Bit 3 - Reserved

Not used, forced to a zero

Bit 2 - Aborted Command

This bit is set if a command was issued while the READY or WRITE FAULT conditions exist. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 - TKØØØ Error

This bit is set only by the restore command. It indicates that the track zero has not been found after the issuance of 1Ø24 stepping pulses.

Bit Ø - Reserved

Not used, forced to a zero.

Write Precomp Cylinder:

This register is used to define the cylinder number where the RWC (Reduced Write Current) line is asserted.

7 6 5 4 3 2 1 Ø

Cylinder Number 4

The value (Ø-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted.

Sector Count:

This register holds the number of sectors that are needed to be transferred to the buffer.

7 6 5 4 3 2 1 Ø

Number of Sectors

This register is used during a multiple sector Read or Write Command.

The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

Sector Number:

This register holds the sector number of a desired sector.

7 6 5 4 3 2 1 Ø

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from Ø to 255.

Cylinder Number Low:

This register holds the least significant 8 bits of the desired cylinder number.

7	6	5	4	3	2	1	Ø

LS Byte of Cylinder Number

It is used in conjuction with the cylinder number high register to specify a range of Ø to 1Ø23.

Cylinder Number High:

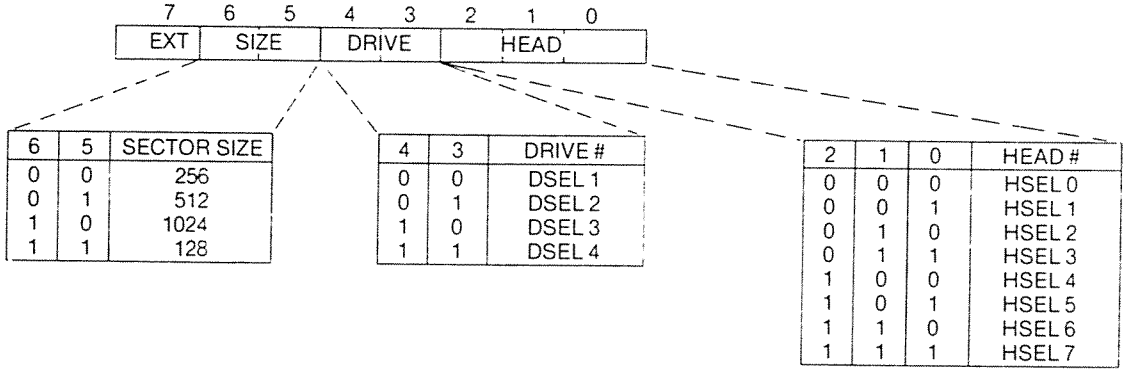
This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	Ø
X	X	X	X	X	X	Bit 9	Bit 8

X = Don't Care

SDH BYTE:

This register contains the desired sector size, drive number and head number paramters. The format is:



6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Bit 5 - Write Fault

This bit reflects the state of the Write-Fault signal from the disk drive. Whenever the Write fault goes high, an interrupt will be generated. Write fault is also latched like Ready.

Bit 4 - Seek Complete

This bit reflects the state of the Seek Complete line from the disk drives. Certain commands will pause until Seek Complete is true.

Bit 3 - Data Request

This bit reflects the state of the BDRQ (pin 36 of WD1Ø1Ø) line. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command.

Bit 2 - Reserved

Not used. This bit is always forced to a zero.

Bit 1 - Command in Progress

When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host.

Bit Ø - Error

This bit is set whenever any bits in the error register are set. It is the logical 'OR' of the error register and may be used by the host to quickly check successful completion of a command.

Command Register:

This write -only register is loaded with desired command.

7 6 5 4 3 2 1 Ø

Command

The commands begin to execute immediately upon loading. This register should not be loaded while the BUSY or CIP bits are set in the status register. The HDBINTRQ* signal if caused by INTRQ from WD1Ø1Ø will be cleared by a WRITE to The Command Register.

Instruction Set

The WD1ØØØ-TB1 will execute six commands prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

Command	7	6	5	4	3	2	1	Ø
Restore	Ø	Ø	Ø	1	R_3	R_2	R_1	$R_Ø$
Seek	Ø	1	1	1	R_3	R_2	R_1	$R_Ø$
Read Sector	Ø	Ø	1	Ø	I	M	Ø	Ø
Write Sector	Ø	Ø	1	1	Ø	M	Ø	Ø
Scan ID	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø
Write Format	Ø	1	Ø	1	Ø	Ø	Ø	Ø

R3- RØ Rate Field (For 5MHZ WCLK)

Ø	Ø	Ø	Ø	35µs
Ø	Ø	Ø	1	Ø.5ms
Ø	Ø	Ø	1	1.Øms
Ø	Ø	1	1	1.5ms
Ø	1	Ø	Ø	2.Øms
Ø	1	Ø	1	2.5ms
Ø	1	1	Ø	3.Øms
Ø	1	1	1	3.5ms
1	Ø	Ø	Ø	4.Øms
1	Ø	Ø	1	4.5ms
1	Ø	1	Ø	5.5ms
1	1	Ø	Ø	6.Øms
1	1	Ø	1	6.5ms
1	1	1	Ø	7.Øms
1	1	1	1	7.5ms

M = Multiple Sector Flag

M = Ø Transfer 1 Sector

M = 1 Transfer Multiple Sectors

I = Interrupt Enable

I = Ø Interrupt BDRQ time

I = 1 Interrupt at end of Command

If the I flag is set, the HDBINTRQ* is made active coincident with HDBDRQ*, indicating a transfer of Data is required by the host. If I = Ø, the HDBINTRQ* will occur at the end of the command.

An optional M flag may be set for multiple sector transfers. When M = Ø one sector is transferred and the Sector Count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1ØØØ-TB1 decrements the Sector Count register and increments the Sector Number register. The next logical sector will be transferred, regardless of the interleave. If at any time prior to the transfer of the last sector, on board sector is full, HDBDRQ* will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the remaining sectors in this multiple sector read command.

Write Sector

The Write Sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1ØØØ-TB1 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a Seek Command takes place.

After Seek Complete is found to be true (with or without an Implied Seek), the BDRQ signal is made active and the host proceeds to load the buffer. When BRDY line goes high, the ID field with the specified cylinder, head and sector size is searched for. Once found, the Write Gate signal is raised and the data is written to the disk. If the ID field cannot be found within eight (8) revolutions, the ID not found bit is set and the command is terminated.

During a multiple sector write operation (M flag =1), the sector number is decremented and the sector count register is incremented. If the BRDY line is low after the first sector is read out of the buffer, the WD1Ø1Ø chip will continue to read data out of the buffer for the next sector. If BRDY is high, the WD1Ø1Ø chip will raise BDRQ and wait for the host to place more data in the buffer.

Scan ID

The Scan ID command is used to update the head, sector size, sector number and cylinder register.

After the command is loaded, the Seek Complete line is sampled until True. The Ready or Write Fault lines are also checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, Cylinder and Sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, retries are attempted up to eight (8) revolutions to find an error-free ID field.

There is no Implied Seek with this command and the buffer is left undisturbed.

Write Format

The Write Format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for an additional parameter information instead of sector data.

Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A H'ØØ' is normal; a H '8Ø' indicates a bad block mark for that sector.

The second byte indicates the logical sector number to be recorded. Using this scheme, sections may be recorded in any interleave factor desired. When Write Enable is active and the target register on WD1ØØØ-TB1 board is selected, the host may write data to the selected register.

Restore Command

The Restore Command is usually used on a Power-Up condition. The actual stopping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1ØØØ-TB1 waits for the Seek Complete line to go active before issuing the next pulse. If after 1Ø24 stepping pulses, the TKØØØ error bit in the error register is set the command will terminate with an interrupt request. An interrupt will also occur if the Write Fault goes active or the DRDY goes inactive at any time during execution.

The rate field specified (R3-RØ) is stored in an internal register for future use in Commands with implied Seeks.

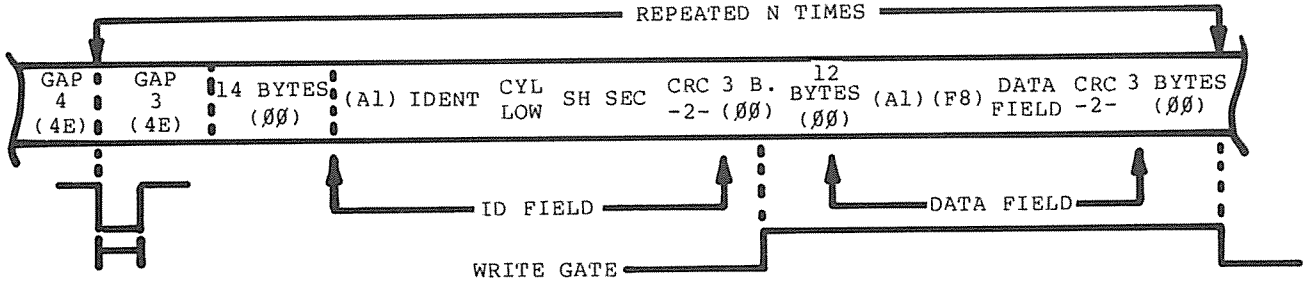
Read Sector

The Read Sector command is used to transfer one or more sectors of data to the disk. Upon receipt of this command, the WD1ØØØ-TB1 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and a Seek takes place.

After Seek is completed, the search for an ID field occurs. The WD1ØØØ-TB1 must find an ID with the correct cylinder, head sector size and CRC within eight revolutions; else the appropriate error bits will be set and the command terminated. When the proper ID field is found, a data address mark must be found within 15 bytes of the end of the ID field. If not, eight retries are performed with the ID-NOT-FOUND error bit set and the command terminated. The remaining memory in the sector buffer may be filled with any value; so BRDY is generated telling WD1Ø1Ø to begin formatting the track.

As implied Seek is also in effect on this command, if the cylinder registers differ from the internal cylinder position. The Sector Count register is used to hold the total number of sectors to be formatted (FF =255 sectors), while the sector number register holds the number of bytes to be used for Gap 1 and Gap 3 (H '4E' is used). The data field is filled with H 'FF' and CRC is automatically generated and appended unless the extension bit is set in the SDH register. After the last sector is written, H '4E' is filled until index.

Figure 5 shows the format that the WD1ØØØ-TB1 will write on the disk.



NOTE:

1) When MSB of head byte = 1, bad block is detected.

2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.

3) Write Gate turn-off is 3 bytes after the Data Field's CRC bytes.

4) 12 bytes of zeros are re-written on a Data Field update.

5) The 2 LSB's of the IDENT byte are used for cylinder sign.

   FE = Ø to 255 cylinders
   FF = 255 to 511 cylinders
   FC = 512 to 767 cylinders
   FD = 768 to 1Ø23 cylinders

6) GAP 3 length is programmable and may range from 3 bytes to 255 bytes.

9/ Troubleshooting the Power Supply -Primary Drive
Section 1

Equipment for Test Set-Up

1. Isolation Transformer (minimum of 5ØØ VA rating)-

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 5ØØ VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. Ø-14Ø Variable Transformer (Variac)-
   Used to vary input voltage. Recommend 1Ø Amp, 1.4 KVA rating minimum.

3. Voltmeter-
   Needed to measure DC voltages to 5Ø VDC and AC voltages to 2ØØ VAC. Recommend two digital multimeters.

4. Oscilloscope-35 MHZ (6Ø MHZ preferred)
   Need X1Ø probe.

5. Load Board with Connectors-
   See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

6. Ohmmeter

Set-Up Procedure

Set-up as shown in Figure 6. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 5Ømv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of Section III for test points within power supply.

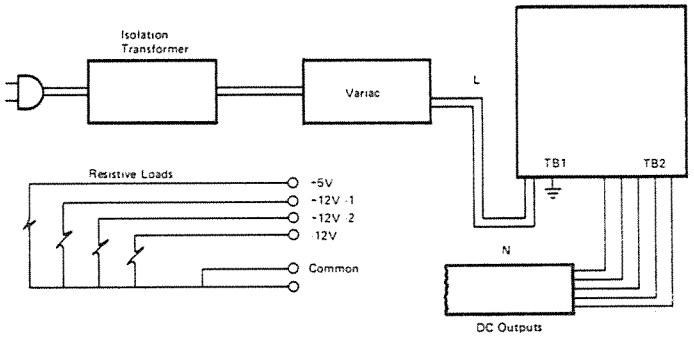


Figure 6. Test Set-Up

Section II

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

OUTPUT	MIN LOAD	LOAD RESISTANCE	SAFE LOAD POWER	MAX LOAD	LOAD RESISTANCE	LOAD LOAD POWER
+ 5V	1.35A	3.7 ohms	12.5 watts	4.0A	1.25 ohms	50 watts
+12V-1	0.40A	30 ohms	10 watts	2.1A	5.7 ohms	50 watts
- 12V-2	0.60A	20 ohms	15 watts	1.5A	8 ohms	35 watts
- 12V	0.0 A	1K ohms	1 watt	0.1A	120 ohms	3 watts

Table 6. Load Board Values

Start-Up

Load power supply with minimum load as specified on Table 6. Bring power up slowly with Variable Transformer while monitoring +5 output with scope and DVM. Supply should start with approximately 4Ø-6Ø VAC applied and should regulate when 9Ø VAC is applied. If output has reached +5 volts, do a performance test as shown in Section IV. If there is no output, refer to Section III.

Section III

No Output

General

When the AC input is applied to the L & N connections and the power does not produce an output, and power switch is on, one or more components have failed. A no output fault condition is most likely caused by a shorted/open component on the primary side but may also be caused by a short on the secondary. To determine the cause follow the steps below.

A. Check Fuse
If fuse is blown, replace it, but do not apply power until the cause of failure is found.

B. Preliminary Check on Major Primary Components
Check diode bridge (DBl), power transistor (Q2), and catch diode (D3) for shorted junctions. If any component is found shorted, replace it.

C. Preliminary Check on Major Secondary Components.
Using ohmmeter from output common to each output, with output loads disconnected, check for shorted rectifiers or capacitors. If +12V output is shorted, also check crowbar SCR (SCRl).

D. Check for B+ with the fuse intact.
Connect power supply and attach XlØ scope probe ground to the anode of (Dl). Slowly turn up power and check for B+ on end of Rl4 nearest the transformer. With imput at 95 VAC, this point should be between 26Ø-27Ø VDC. If this is not correct, check resistor and and DBl.

If Rl4 is open it was most likely caused by a shorted component that is fed power by Rl4. Check the following components for proper operation (Q2, Ql, Dl, D36).

E. Check Q2 Waveforms

Using X1Ø probe on heat sink of Q2, check collector waveform. Transistor should be switching, correct waveform is shown in Figure 7. If this is not present, check for open junction on Q2. If OK check to see if base voltage is being supplied to Q2, it should be .7V. If it is not present, check components (L3, Q1, D1, and R4).

Section IV

Low Output

A. All outputs are low.
If all outputs are low at the same time, check to ensure that the voltage selection jumper is in the proper position.

B. +5V AND +12V -2 outputs
The power supply regulates off of the +5V and +12V -2 outputs. If these outputs are low, it could cause the others to be low. If so, adjust +5V and +12V -2 outputs by removing or adding R27 and R28.

C. If any one output is not present, first check the rectifier associated with that output and then the rest of the components in the circuit and the solder joints on the PCB.

Section V

Crowbar

If the crowbar is not operating, Check Z1, and SCR1. If the crowbar is not triggering within the specified limits change Z1.

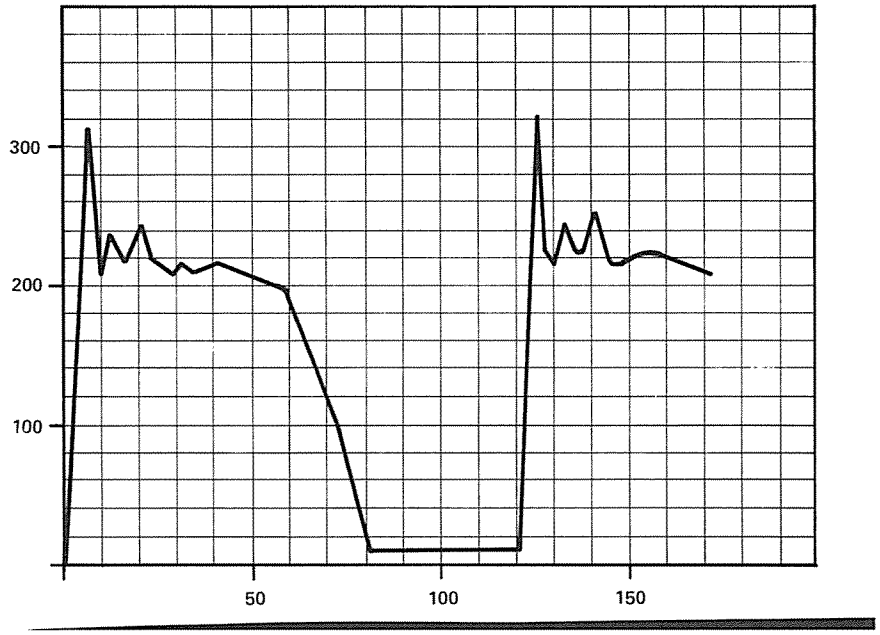


Figure 7. Q2 Collector Waveform

Section VI

Performance Test

Each of these test conditions should be set-up and noted to be within the limits. If the power supply does not pass the above tests, refer to Section IV and V.

Astec Power Supply (Primary Drive)
Operating Characteristics

		Min	Typ	Max	Units
Vin Range					
Input Select 115V		90	115	127	Vrms
Input Select 230V		200	230	253	Vrms
Line Frequency		47	50/60	63	Hz
Output Voltages	V1 +5V	4.95	5.1	5.25	Volts
	V3 +12V	11.4	12	12.6	Volts
	V4 -12V	-11.4	-12	-12.6	Volts
Output Current	V1 +5V	2.50		5.0	Amps
	V3 +12V	.75		2.0	Amps
	V4 -12V	.005		.10	Amps
Ripple Voltages	V1 +5V			50	mV
	V3 +12V			120	mV
	V4 -12V			120	mV
Efficiency		70			%
Hold Up Time					
Full Load, Low Line		10			mSec
Full Load, Nom Line		16			mSec
Over-Voltage Protection		5.80		6.80	Volts

Troubleshooting the Power Supply -Secondary Drive
Section 1

Equipment for Test Set-Up

1. Isolation Transformer (minimum of 5ØØ VA rating)-

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 5ØØ VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. Ø-28Ø Variable Transformer (Variac)-
   Used to vary input voltage. Recommend 1Ø Amp, 1.4 KVA rating minimum.

3. Voltmeter-
   Needed to measure DC voltages to 5Ø VDC and AC voltages to 4ØØ VAC. Recommend two digital multimeters.

4. Oscilloscope-
   Need X1Ø probe.

5. Load Board with Connectors-
   See Table 7 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

6. Ohmmeter

7. Wattmeter

Set-Up Procedure

Set-up as shown in Figure 8. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 5Ømv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of Section III for test points within power supply.

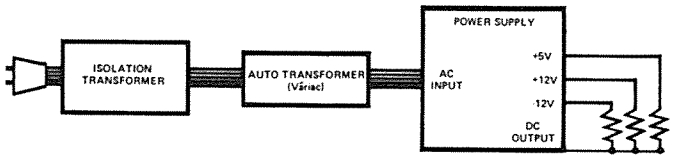


Figure 8. Test Set-Up

Section II

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

LOAD BOARD VALUES

OUTPUT	MIN LOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5	0.45A	11.11 ohm	5W	2.5A	2 ohm	25W
+12	1.3A	0.40 ohm	8W	2.02A	24.24 ohm	50W
-12	0	0	0	0	120 ohm	2W

Table 7. Load Board Values

Start-Up

First note the position of the input voltage select wire. This wire can be found at the end of PCB opposite the input/output connectors. Make sure the wire is in position corresponding to your test set-up 23ØV position if you are using 115V input. For the balance of this troubleshooting section we will assume 23ØV operation. If you prefer 115V operation divide applicable values in half.

Load power supply with minimum load as specified in Table 7. Bring power up slowly with Variable Transformer while monitoring +5 output with scope and DVM and input with DVM and wattmeter. If the wattmeter shows significant power with low AC power being applied, shut down and refer to Section III.. Supply should start with approximately 8Ø-12Ø VAC applied and should regulate when 19Ø VAC is applied. If output has reached +5 volts, do a performance test as shown in Section IV. If there is no output, refer to Section III. For 12Ø VAC use divide 23Ø VAC voltages by two.

Section III

No Output

A. Check Fuse
If fuse is blown, replace it, but do not apply power until the cause of failure is found.

B. Preliminary Check on Major Primary Components
Check thermistor (R1), diode bridge (DB1), power transistor (Q2), and catch diode (D3) and turn-off transistor (Q1), emitter resistor (R1Ø), and diode (D1) for shorted junctions. If any component is found shorted, replace it.

C. Preliminary Check on Major Secondary Components.
Using ohmmeter from output common to each output, with output loads disconnected, check for shorted rectifiers or capacitors. If +12 output is shorted, also check crowbar SCR (SCR1) and zener (Z1).

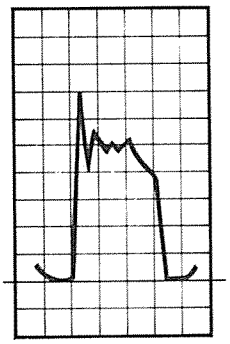
D. Check for B+

Setup power supply and attach X1Ø scope probe ground to end of R11 closest to input capacitors. Slowly turn up power and check for B+ on the (+) terminal of the diode bridge (DB1). With input at 95 VAC, this point should be between 12Ø-14Ø VDC. If this is not correct, check fuse, thermister (R1), DB1, and if necessary, check R2, D3, and finally input capacitors C6 and C7.

E. Check Q2 Waveforms

Using X1Ø probe on the case of TØ3 package of Q2, check collector waveform. Transistor should be switching, correct waveform is shown in Figure 9. If this is not present, check for shorted junction on Q2.

If OK check the base waveform. Base of Q2 is the uppermost of the two center leads on the back of Q2 heat sink. The correct waveform is shown in Figure 1Ø. If this waveform is not present, check L3, Q1, and D1, and secondary components Q3, D11, D12, D5, and L4. If any of the semiconductors are found shorted, or inductors open, replace them.



50 V/DIV
5 μsec/DIV

Input – 120VAC
Loads – +5 @ 2A
+12 @ 1A
-12 @ 0.1A

Figure 9. Q2 Collector Waveform

1.0 V/DIV
5 μsec/DIV

Input and Loads same as above.

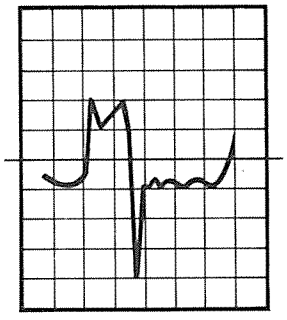


Figure 1Ø. Q2 Base Waveform

Section IV

Performance Test

Each of these test conditions should be set-up and noted to be within the limits.

Test	Input	+5 Load	+12 Load	12 Load
1	95VAC	Max	Max	Max
2	128VAC	Max	Max	Max
3	120VAC	Max	Min	Min
4	128VAC	Min	Min	Min
5	95VAC	Min	Min	Min

VOLTAGE AND RIPPLE SPECIFICATION

OUTPUT	MIN	MAX	NO LOAD	RIPPLE
+5	4.75V	5.25V		50mV P-P
+12	11.40V	12.60V		150mV P-P
12	11.00V	15.00V		150mV P-P

Astec Power Supply (Secondary Drive)
Operating Characteristics

		Min	Typ	Max	Units
Vin Range					
Input Select 115V		95	115	135	Vrms
Input Select 230V		180	230	264	Vrms
Line Frequency		47	50/60	63	Hz
Output Voltages	+5V	4.75	5	5.25	Volts
	+12V	11.4	12	12.6	Volts
	-12V	-11	-12	-15	Volts
Output Current	+5V	.45		2.5	Amps
	+12V	.75		2.0	Amps
	-12V	.005		.10	Amps
Load Regulation (measured by varying load on considered output from typ to either min or max rated load)	+5V	5		5	%
	12V	-5		5	%
	-12V	-8.3		25	%
Ripple Voltages	+5			50	mV
	12V			150	mV
	-12V			150	mV
Efficiency		65			%
Over-Voltage Protection		5.80		6.80	Volts

Tandy 65W Power Supply

Basic Principle

A switching power supply circuit employs a high-speed semiconductor switch to control the storage and release of electrical energy in an inductor and provide regulated DC output voltages with a minimum loss of energy in heat-dissipating elements. There are several schemes for achieving this result which differ primarily in the arrangement of the basic circuit elements. These elements include a switch, an inductor, a rectifier, a capacitor and a DC voltage source.

An arrangement well-suited for economical power supplies with rated power outputs under 1ØØ watts is the FLYBACK CONVERTER shown in Figure 11. The waveforms in Figure 12 are used to describe the operation of the Flyback Converter circuit. For the purpose of this discussion we will assume that the duration of the "ON" time equals the duration of the "OFF" time and Vo = rated output voltage.

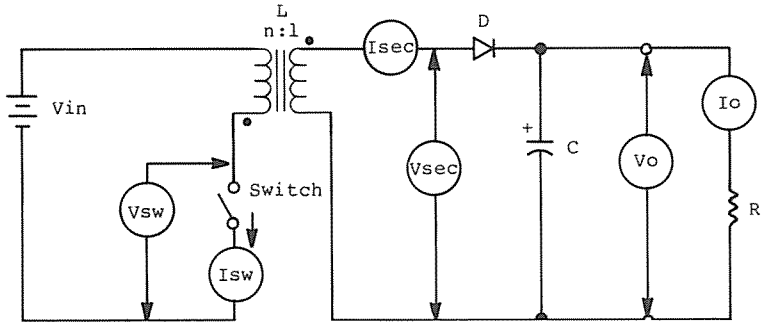


FIGURE 11. BASIC FLYBACK CONVERTER

When the switch is closed (ON) at time ta, Vin is impressed across the primary winding of inductor L and the current Isw increases linearly from zero until the switch opens (OFF) at time tb. Note that Isec is zero while the switch is closed. This is because Vsec is negative with respect to Vo thus reverse-biasing diode D. Note that Vsw is also zero while the switch is closed.

When the switch opens at time tb, the magnetic field of L instantly collapses and reverses polarity. At this moment, Vsw is equal to Vin plus the voltage across L just before

the switch opened (also equal to Vin). Therefore, at the instant the magnetic field reverses polarity, Vsw = 2Vin.

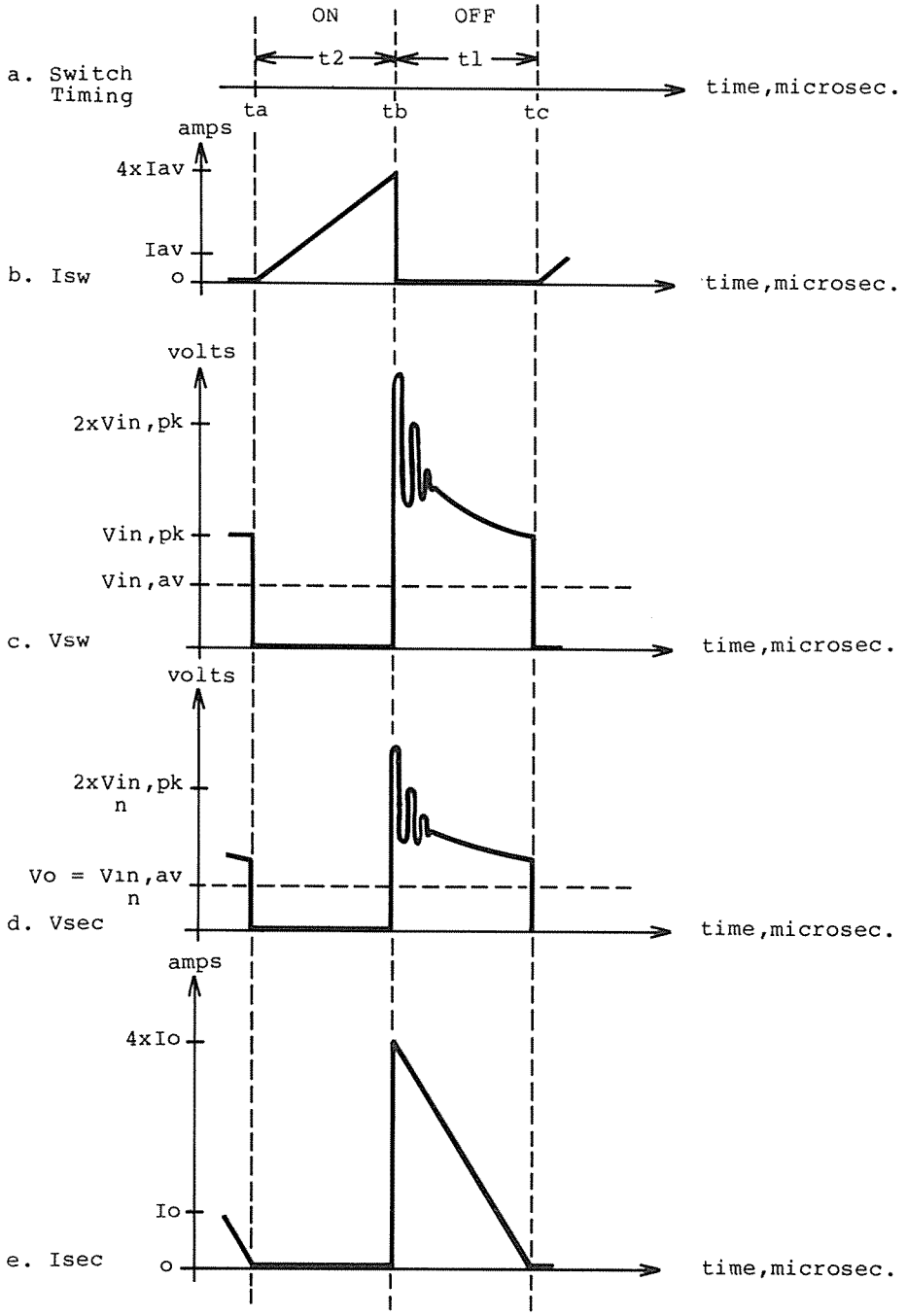


Figure 12. Waveforms for Figure 11.

During the interval when the switch is open (tb to tc), the secondary voltage, Vsec, is a replica of the primary voltage Vsw. Diode D is now forward biased due to the polarity of the inductor windings and because the turns ratio, n, is such that:

$$Vsec \times n > Vo$$

This biasing replenishes the charge in capacitor C that was delivered to the load R during the ta-tb interval. This is the "flyback" interval and is so named because the inductor releases the energy stored in its magnetic field while the switch is OFF.

Several other facts are illustrated by the waveforms of Figure 12. First, the voltage across the switch Vsw decays exponentially from 2Vin to Vin during the "OFF" interval. This is because the inductor and the switch timing are adjusted to transfer all of the energy that was stored in the inductor while the switch was ON, into the secondary while the switch is OFF. (Observe that Isec DECREASES linearly with time to zero at the end of the "OFF" time period.) This is known as resetting the core. Thus, at time tc when the switch is ready to turn on again, the DC input voltage Vin is again available to charge the inductor. Also at this time, all currents in the inductor are zero.

Second, since we have assumed that Isw increases linearly with time and that the ON and OFF time periods are equal (50% duty cycle), the average current in the primary, Isw (av), is 1/4 the peak current Isw. Also, the average current in the secondary, which is equal to the load current Io, is 1/4 the peak current in the secondary.

Third, the turns ratio is set by the ratio of the average primary voltage (Vsw) over a full cycle at its lowest value to the maximum permissible output voltage, Vo. The lowest Vsw value occurs at low AC line and maximum output load. In practice, the actual turns ratio, the ratio of peak-to-average voltages and currents, and the duty cycle may be adjusted to compensate for circuit losses.

Fourth, notice the ringing or oscillation that appears on the peak portion of Vsw and Vsec. This oscillation occurs at the resonant frequency of the leakage inductance of the inductor L and the parasitic capacitance of the circuit. The parasitic capacitance includes the interwinding capacitance of the inductor and stray capacitance of the switch. If this oscillation is not damped by a suitable means, the peak voltages may easily exceed the breakdown rating of the switch or the insulation in the inductor.

Block Diagram

The basic circuit illustrated in Figure 11 can be divided into three functional blocks: Input DC supply, primary, and secondary. To make use of this model, we need to expand it to provide control for the switch timing and to include sufficient circuitry to satisfy performance and reliability specifications. The complete block diagram is shown in Figure 13.

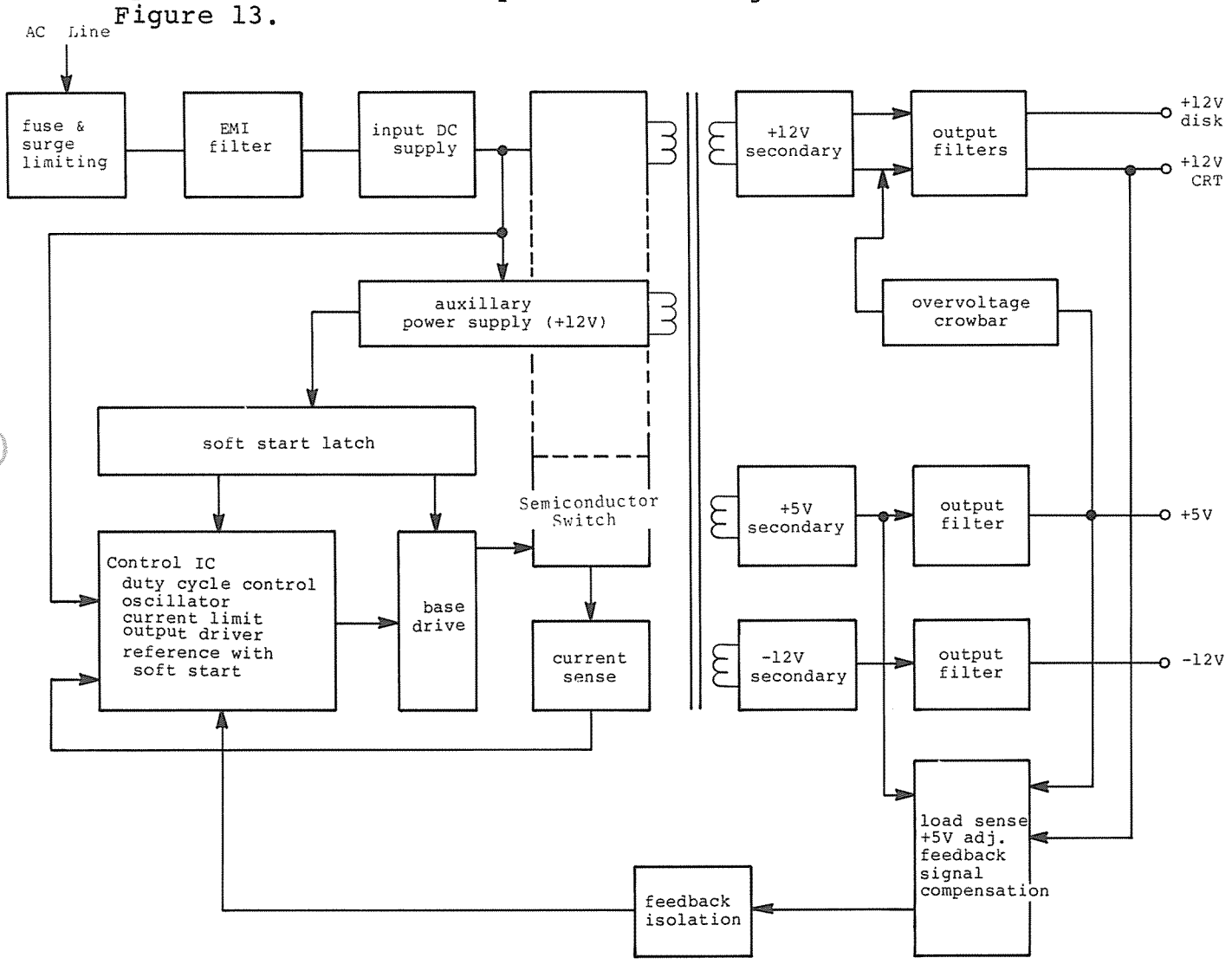


FIGURE 13. BLOCK DIAGRAM

The other blocks provide additional output voltages, add safety or protective features, reduce circuit noise, and

develop signals for use by the control section. The control section continously operates the bipolar transistor switch and varies the proportion of ON time to OFF time in response to changes in the AC input line voltage or output load current. This is accomplished by feeding back a signal from the output terminals that instructs the control section to increase or decrease the ON time to compensate for a change in the output voltage.

The DC voltage supply to the control section is controlled by the latch circuit when AC power is first applied to the power supply. A built-in timing circuit allows the input DC supply filter capacitor to become fully charged before power is applied to the control section. After the control section circuit starts and secondary voltages reach their regulated output levels, the auxiliary power supply provides the required DC voltage to operate the control section. The latch is reset when the current limit or under-voltage sensors operate, thus removing DC voltage to the Control IC.

There are four secondary or output voltages in addition to the auxiliary supply: +5.Ø5 volt, +12 volt CRT, +12 volt Disk, and -12 volt. The +5.Ø5 and +12 DISK voltages are regulated by the control circuit response to the frequency compensated feedback control signal which comes from the load sense section. Since the load sensing occurs on the secondary side, an optical coupler circuit is necessary to provide safety isolation between the primary side common ground and the secondary side common ground.

All the secondary voltages, including the auxiliary +12 voltage, share the same magnetic flux linkage in the transformer core and are controlled by the flyback inductor. Any change in secondary load currents cause a change in the shared magnetic flux. This change in the flux of the inductor sets up an EMF (electromotive force) which causes a flux in opposition to the one which resulted from the change in load current. Thus, the original change tends to be counteracted and the current delivered to the load remains constant.

The output filters reduce the remaining ripple voltage components of the AC line and switching frequencies to levels low enough to prevent interference with the circuits operated by the supply. Switching frequency components that

The overvoltage crowbar senses an abnormal rise in the +5.1 volt output and short-circuits the voltage line to the common secondary ground, thus tripping the current limiting circuit which finally shuts down the supply.

The surge limiter at the AC line input prevents the input filter capacitor in-rush current surge from exceeding component ratings or unnecessarily tripping external fuses.

Technical Specifications

Environment:

Temperature;	Operating	Ø to 5Ø C (32 to 122 F)
	Storage	-4Ø to 85 C (-4Ø to 185 F)
Humidity;	Operating	85% r.h. @ 35 C (95 F) max.
	Storage	95% r.h. @ 55 C (131 F) max.

Input Voltage:
9Ø to 135 VAC rms, 47 to 63 Hz

Input Surge Current:
48 amps max.

Efficiency:
7Ø% min. at full load with 115 VAC rms input

Output Voltages:
V1, +5.Ø5 VDC
V2, +12 VDC CRT
V3, +12 VDC DISK
V4, -12 VDC

Output Power:
continuous 65 watts max.

Output Current:

		Load	
	Output	Min.	Max.
Condition 1 (Model III use)	V1	1.35 A	4.Ø A
	V2	Ø.6Ø A	1.5 A
	V3	Ø.4Ø A	2.1 A
	V4	Ø.ØØ5 A	Ø.1Ø A
Condition 2 (Hard Disk use)	V1	2.5 A	5.Ø A
	V3	Ø.75 A	2.Ø A*
	V4	Ø.ØØ5 A	Ø.1Ø A

*NOTE: V2 and V3 connect in parallel to provide the V3 output. The V3 output will support a 5.Ø A peak load which decays to 1.Ø A in approx. 8 seconds. V1 and V3 must be within specified regulation when this surge decays to 4.Ø A.

Output Ripple Voltage:

V1	(5.Ø5 VDC)	5ØmV p-p
V2	(+12 VDC)	15ØmV p-p
V3	(+12 VDC)	15ØmV p-p
V4	(-12 VDC)	15ØmV p-p

NOTE: Ripple is the composite 1ØØ/12Ø Hz ripple due to the line, plus the high frequency ripple due to the power oscillator. Common mode noise which may be observed due to oscilloscope connections should be ignored.

Output Voltage Regulation:

After initally setting V1, output voltage tolerances under all conditions of rated line, load, and temperature should remain within the following limits:

V1	(+5.Ø5 VDC)	+/- 3%
V2	(+12 VDC)	see *NOTE
V3	(+12 VDC)	+/- 5%
V4	(-12 VDC)	+25%, -8.3%

*NOTE: a) The initial value of V2 must not change by more than +/- 1ØØmV under the following load conditions of V3:
-- A step increase in output current from Ø.4 A (initial condition) to 2.4 A, decaying within 6Ø msec to 2.1 A.
-- A step decrease in output current from 2.1 A (initial condition) to Ø.4 A.

b) V2 output voltage may vary +/- 5% under all other conditions of rated line, load, and temperature as defined in the specification.

Over-Current Protection:

Power supply will shut down before total power exceeds the point where damage would result. No damage will result when any output is short circuited continuously with 1ØØ milliohms or less.

Over-Voltage Protection:

The +5.Ø5 VDC circuit is protected with a "crowbar" circuit with a trip range of 5.8 to 6.8 VDC.

Hold-Up Time at Continuous Max Load:

Nominal Line	16 mSec minimum
Low Line	1Ø mSec minimum

Theory of Operation

The basic operating principles of a flyback converter and the necessary functional blocks to form a complete power supply were reviewed in the System Description section. In this part, the operation of each section of the circuit will be analyzed and later these sections will be connected to illustrate the signal flow in the power supply.

AC Input

A conventional bridge rectifier and a filter capacitor are connected directly across the AC line to provide the DC input voltage to the power supply.

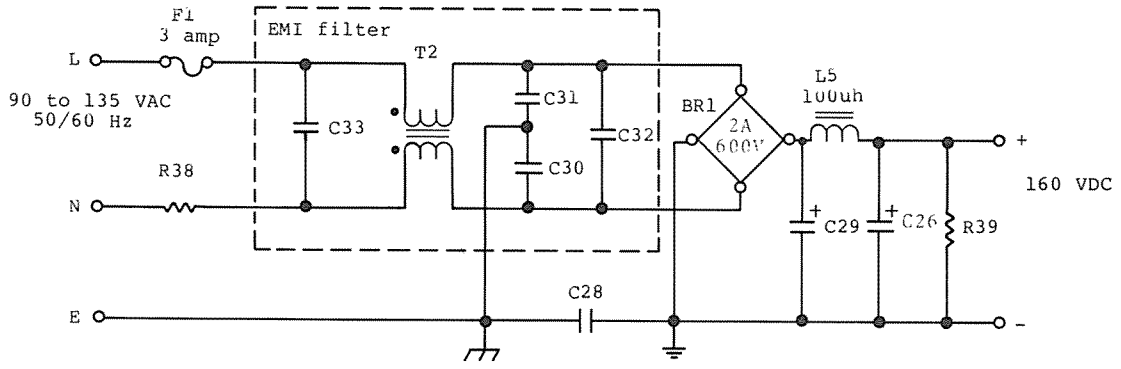


FIGURE 14. INPUT AC SUPPLY

An EMI filter consisting of capacitors C3Ø-C33 and choke T2 are inserted at the input to the rectifier. This filter circuit keeps the high frequency signals generated in the power supply from being conducted into the AC power line. C3Ø and C31 provide a low impedance to the earth ground terminal for signals common to both hot and neutral sides of the AC line. C32 provides a low impedance dissipative path for the RF signal energy which appears across the line. T2 blocks RF signals common to both sides of the line and reflects them back toward the lower impedance elements near the rectifier. T2 also helps block differential (across-the-line) signals by using the EMF set up by the signal current on one side of the line to oppose the signal current flowing in the other side. C33 serves as a

transient bypass capacitor to protect the power supply from large transient voltages that appear on the AC power line. C33 also improves the efficiency of the RFI filter choke T2 by terminating the line in a low impedance to absorb and dissipate any remaining differential RF energy.

R38 is a negative-temperature-coefficient-thermistor which limits the turn-on surge current of the power supply filter capacitor C29. The resistance of this thermistor when "cold" is approximately 1Ø ohms. As the filter capacitor charges toward the peak value of the AC input voltage, it draws less current from the line. At the same time, the heating effect of the current flowing in the thermistor causes its resistance to decrease until it reaches its rated "hot" resistance of less than 1 ohm. As you can see, the thermistor dissipates very little power when the power supply is in operation. The thermistor is designed to cool rapidly enough, during power loss or turn-off, to limit the turn-on surge after only a few seconds cool-down.

The fuse, a fast acting 3.Ø amp unit, is selected to ignore the short term turn-on surges, but open quickly in the event of an abnormally high current that would result from a component failure in the DC input supply or current limiting circuits.

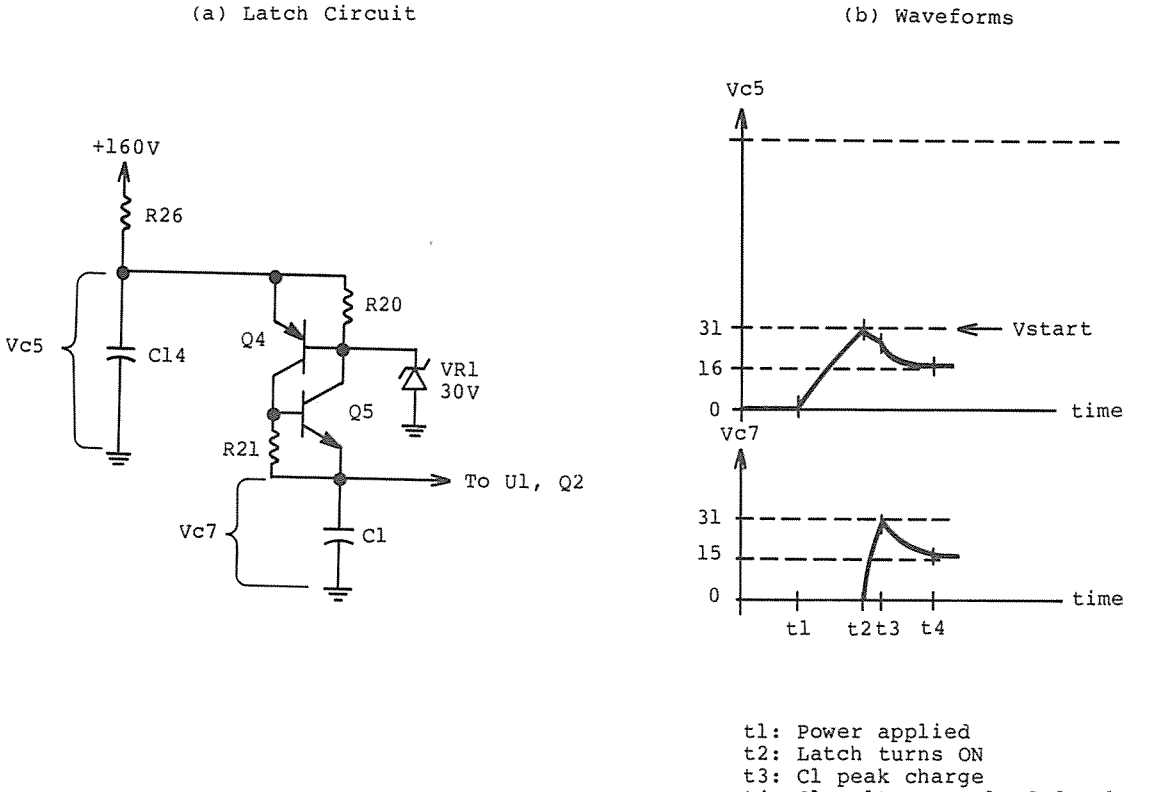
Auxiliary Power Supply

The auxiliary power supply is operational when the main supply is on and not in a shut-down condition. This power supply consists of winding 2-3 on T1, half-wave rectifier CR4, and filter capacitor C14. The voltage output is approximately +15 volts under normal conditions but momentarily reaches about +31 volts during start-up.

Kick Start Latch

Start up of the circuit is initiated by the kick start latch. This latch is shown in simplified form in Figure 15a along with the accompanying waveforms in Figure 15b. When power is applied, C14 charges toward Vin = +16Ø volts through R26 with a time constant of approximately RC or 37.5 seconds. However, as we'll see, the kick start latch turns on in 2 or 3 seconds, the time required for the voltage across C14 to reach 3Ø + Vbe4 = 3Ø.7 volts. At this point Q4 turns on and develops a bias across R21 which turns on Q5.

Referring to Figure 15b, as C14 dumps its charge into C1 beginning at time t2, the voltage across C14 starts to decrease toward a level that will be determined by the load composed of U1 and the base drive circuit. Notice that the voltage across C1 momentarily approaches the full 31 volts at time t3 before it drops down under load to about +15 volts at time t4.



t1: Power applied
t2: Latch turns ON
t3: C1 peak charge
t4: C1 voltage at loaded value
Vin = 160 volts

FIGURE 15. KICK-START LATCH

With C1 charging rapidly through the low resistance of a saturated Q4 via Vbe5, the reference supply inside U1 develops its 5.Ø volt output when the voltage across C1 exceeds about 8 volts. At this point, the supply has not quite yet started, but U1 has a DC supply at pin 1Ø. All that remains is to start up the pulse generator so that the supply operates and replenishes the charge in C14 on each cycle, thus maintaining a DC source for U1 of about +15 volts. Completion of the start-up sequence occurs when the soft start circuit, described in the next section, has started the pulse generator.

Control Section

The control section consists of the control IC, the primary half of the feedback optocoupler U2, and the base drive circuit for the switching transistor. The control circuit IC has three major parts: an internal regulator, a pulse generator, and an error amplifier section.

The internal reference is a regulated +5.Ø DC voltage. This voltage provides the reference voltages for the comparators used in the pulse generator as well as the DC supply voltage for the feedback optical coupler and the internal circuits of Ul except for its output transistors.

The pulse generator section of the control IC has four major parts: (a) sawtooth oscillator; (b) wave-shaping and output circuit; (c) regulating comparator; (d) dead-time comparator. Figure 16 illustrates the sawtooth oscillator and output circuit waveforms and the approximate levels of the DC control voltages applied by the comparators to the wave-shaping logic. The oscillator frequency is set by the values of R3 and C7 shown in Figure 17.

The amplitude of the sawtooth is set at 3.Ø volts (approximately 6Ø% of the 5.Ø volt reference voltage). Whenever the sawtooth voltage, Vosc, exceeds both of the DC control voltages, Vreg and Vdt, the output circuit will be in the ON condition.

The DC control voltage, Vreg, set at a quiescent value by R6 and R9, varies in response to changes in the supply's DC output voltages as sensed by U3 and coupled through U2. Notice that these voltages will vary because of changes in output loading, AC input voltage, and also because of the residual 12Ø Hz ripple component from the main DC supply.

The dead-time control voltage, Vdt, is set at a constant value by R4 and R5 and ensures that the pulse generator "OFF" time will be at least 5Ø% of the sawtooth period. This allows adequate time for the complete transfer of stored energy from the primary to the secondary of transformer Tl as discussed in the section on basic principles.

A concept known as duty cycle was introduced in earlier paragraphs. Duty cycle is defined as the ratio of the "ON" time of the sawtooth cycle to the total length of the sawtooth period. Since the sawtooth has a linear ramp characteristic, the duty cycle is also equal to:

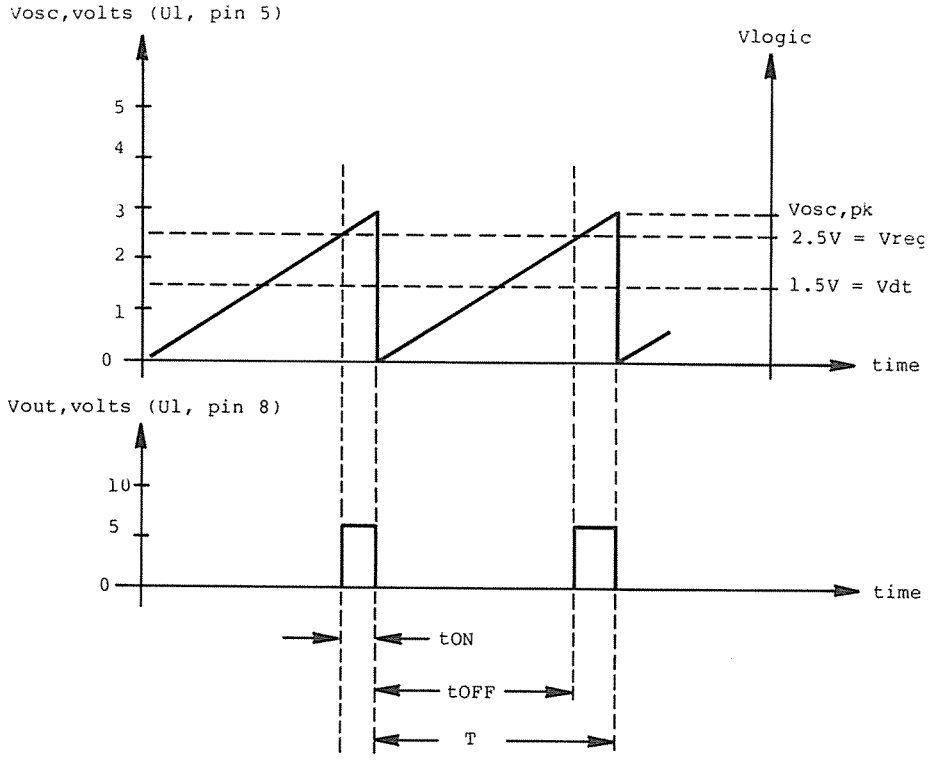
$$\text{duty cycle } d = \frac{V_{osc,pk} - V_{reg}}{V_{osc,pk}} = \frac{t_{on}}{T \text{ period}}$$

There are three possible conditions of the duty cycle:

d = Ø which occurs when either control voltage Vreg or Vdt exceeds the peak value of the sawtooth waveform Vosc

d = 5Ø% which occurs when Vreg is less than Vdt. This happens when the loading on the output of the supply is heaviest and the AC input voltage is at its lowest permitted level (see specifications)

Ø < d <5Ø% which occurs during normal operation.



$\tau \cong$ 25 microsec.

FIGURE 16. OSCILLATOR, PULSE GENERATOR WAVEFORMS

The dead-time control voltage is used in one other important way. Notice the 4.7 ufd capacitor, C2, connected across R4 in Figure 17. When power is first applied to the supply, the voltage across the capacitor is zero. Therefore, Vdt = Vref = 5.Ø volts and no pulses appear at the output because Vdt is greater than Vosc,pk. As C2 charges, Vdt decreases toward 1/2 (Vosc,pk) in a time determined by R5 and C2 as t = 5x15k ohm X 4.7 ufd = 1/3 second. As Vdt decreases past Vosc,pk, very narrow pulses begin appearing at pin 8 of U1. The pulses become successively wider until Vdt is less than Vreg. C2 continues charging until Vdt reaches the final correct value of about 1.5 volts. This action provides the soft start feature of the power supply and allows sufficient time for the DC input supply and latch to reach normal operating conditions before the supply is started. In effect, the load is connected to the supply gradually by the soft start circuit.

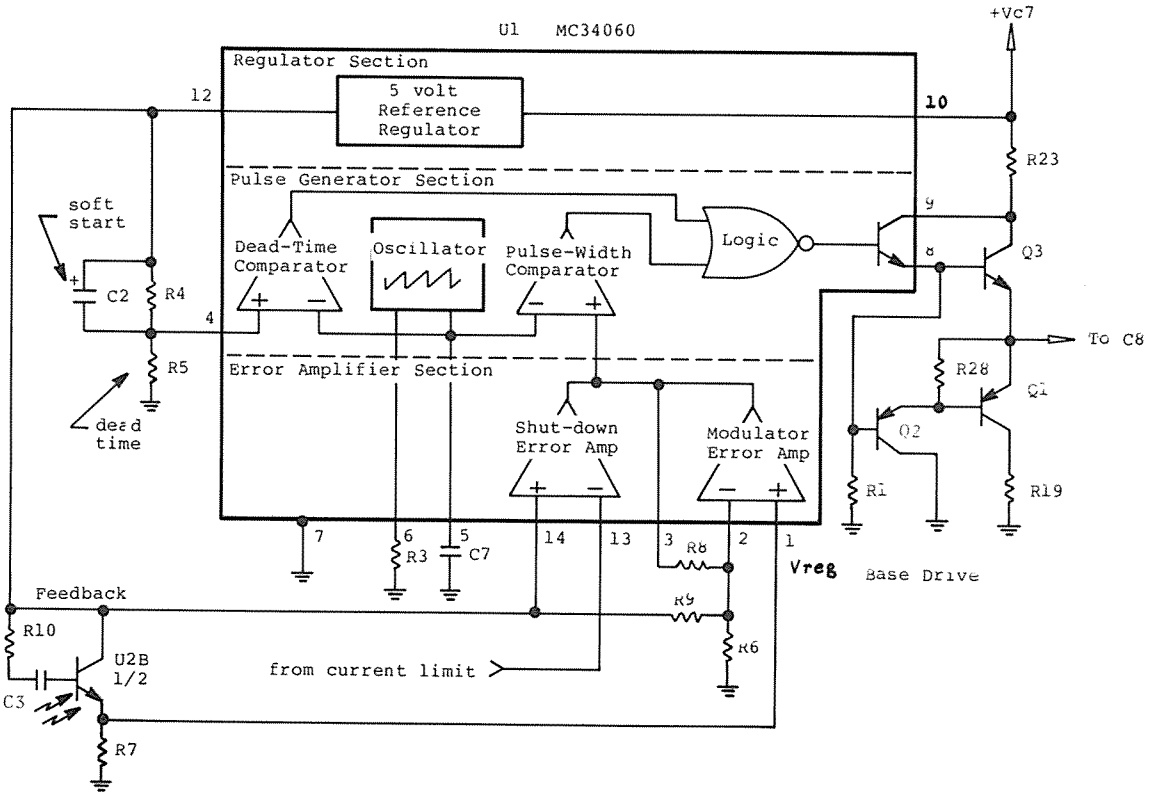


FIGURE 17. CONTROL SECTION

Frequency stability of the sawtooth oscillator is provided by the 2% tolerance and polyester construction of the timing capacitor, C7, and the 1ØØ parts-per-million temperature stability and 1% tolerance of R3. Voltage stability of the DC control voltages is provided by the +/- 2 1/2 percent stability of the 5.Ø volt reference.

The control section consists of two error amplifiers in U1, the primary half of U2, and associated circuitry shown in Figure 17. One of the error amplifiers serves as a regulator or pulse-width modulator which derives the DC control voltage, Vreg, from the signal voltage developed across R7 by the current in U2. This current is a replica of the current developed by U3 in response to the condition of the output voltage at the +5.1v and +12v outputs. This amplifier has a gain of about 1Ø determined by:

$$A = \frac{R8}{R9 \quad R6} = \frac{22k\ ohm}{2.35k\ ohm} = 1Ø$$

The other error amplifier in U1 serves as a shut-down comparator. The positive terminal, pin 14, is set at the +5.Ø volt reference and pin 13, the negative terminal or shut-down pin, is tied to the current limit latch. The output of this error amplifier (equal to Vreg since both error amplifier outputs are tied to the wave-shaping logic) will rapidly increase toward the +5.Ø volt reference when pin 13 drops below 5.Ø volts. Recall that if Vreg exceeds the peak sawtooth voltage, pulses are inhibited and the power supply shuts-down.

Base Drive

Figure 18 illustrates the BASE DRIVE circuitry which turns switching transistor Q7 on and off in response to the output of the pulse generator portion of U1. The "ON" circuit is shown in Figure 18a and the "OFF" circuit is shown in Figure 18b. Waveforms for these circuits appear in Figure 19.

The output transistor of U1 combined with Q3 forms a Darlington pair. This circuit provides the relatively large current necessary (through coupling capacitor C8) to turn on Q7. R23 limits this base current to a value large enough to turn on Q7 quickly, but not so large that it will exceed the ratings of Q3, C8, or the base emitter junction of Q7, or so large that the turn-off time of Q7 is excessive.

As Q3 turns on, C8 charges to approximately +5 volts and Q7 is driven into saturation. Energy is stored in the primary winding of T1 as the collector current of Q7 increases or "ramps up" at a rate determined by the inductance of the transformer primary winding.

When the output transistor of U1 turns off, the emitters of Q1 and Q2 are initially at the +6 volt level determined by the charge on C8, the Vbe drop of Q7, and the drop across R37. Both base-emitter junctions of the Q1-Q2 darlington pair are biased ON and the positive terminal of C8 is clamped to near-ground by the saturating Q1. At this point, C8 still has most of its charge and the base voltage of Q7 is approximately -4.5 volts with respect to ground.

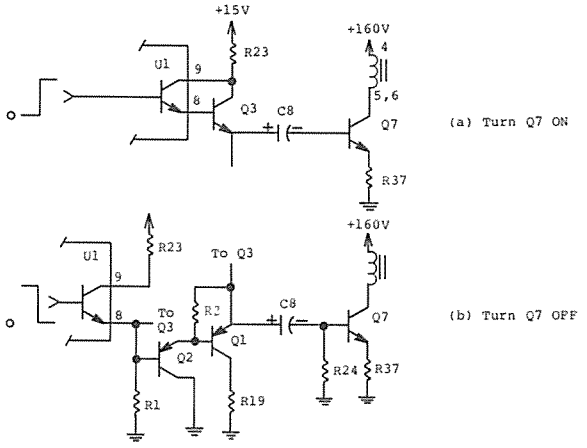


FIGURE 18. BASE DRIVE CIRCUIT

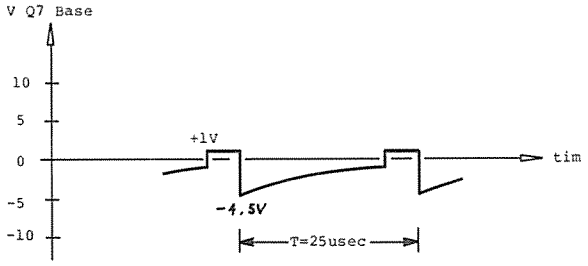


FIGURE 19. Q7 BASE VOLTAGE WAVEFORM

With the strong reverse polarity provided by C8 across the base emitter junction of Q7, the "forward" charge stored in the junction capacitance is quickly swept out and Q7 is turned off. C8 continues to discharge through R24 to

prepare for the next "ON" cycle. R19 limits the initial discharge of C8 while Q7 is turning off.

Notice the symmetry in the base drive circuit and the key role played by C8 in both the turn-on and turn-off sequences. Because of this crucial role in the circuit, this capacitor is specified as a high temperature, low-equivalent-series-resistance component.

Primary Circuit and Current Limit Shutdown

The Primary Circuit

The Primary circuit, shown in Figure 2Øa, functions exactly as described earlier in the "Basic Principle" section. That is, the switch (Q7) is controlled by the base drive waveform developed by the control section.

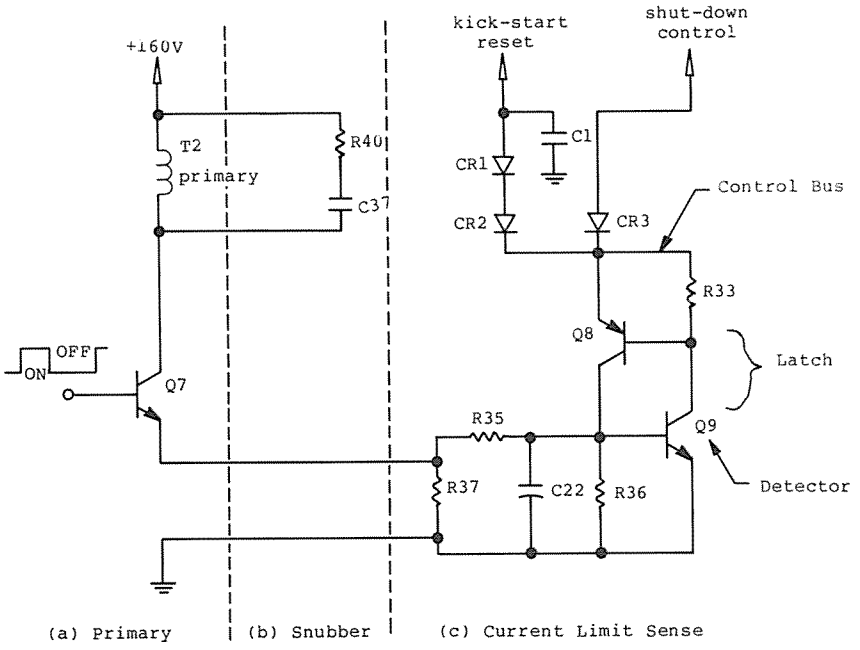


FIGURE 2Ø. PRIMARY SIDE PROTECTION

The Snubber Circuit

Practical transformers cannot couple 1ØØ% of the stored energy from the primary to the secondary since all of the flux from the primary fails to link all the secondary turns. A circuit using this practical transformer behaves as though a small fraction of the primary inductance was not wound on

the core of the transformer, but instead placed apart from the primary and in series with it. This small, separately-acting inductance does not participate in the transformer action and is called the leakage inductance.

If the resonant circuit, consisting of this leakage inductance and the stray capacitance in the adjacent circuit, has sufficient Q (relatively low resistance losses), a damped oscillation will occur in this resonant circuit when the transistor switch opens. The peak value of this oscillation will add to the Vce = 2 x Vin which appears across the transistor switch just after turn-off. The combined peak Vce may exceed the transistor breakdown rating if not damped out by the action of a snubber circuit.

When Q7 turns off, the energy stored in the leakage inductance is transferred to the electric field of the total capacitance of C37 plus stray capacitance. (Since C37 capacitance is much larger than the strays, it dominates in this action and tends to limit the peak value of the Q7 turn-off voltage.) If there were no resistance in this series connection of C37-plus-parasitics and leakage inductance, they would exchange this energy back and forth indefinitely. R4Ø is used to damp this oscillation without excessively slowing the turn-off of Q7, thus effectively snubbing the turn-off voltage spike at the collector of Q7.

Current Limit Circuit and the Shut-Down Sequence

The current limit circuit forces the voltage level at a control pin of U1 to change to a near-zero value very quickly when the current in the transistor switch exceeds a predetermined point. It also removes the supply voltage from the control circuit and resets the kick start latch and soft-start circuits.

The current limit circuit shown in Figure 2Øc has three parts: a control bus, a detector, and a latch. The control bus supplies the operating DC voltage to the current limit circuit. It also conducts the current limit signal to control pin 13 and to the reset point in the kick start latch circuit. Diodes CR2 and CR3 steer this signal.

The normal maximum peak current in switching transistor Q7 is 3 amps. The detector transistor Q8 is biased to turn on by the divider action of R35 and R36 whenever the Q7 peak current through R37 exceeds 4 amps. A low-pass filter, formed by R35 and C22, prevents false detections on transient signals that don't represent an over-current condition.

As soon as Q9 turns on, its collector current develops the turn-on bias for Q8 across R33, and the Q8-Q9 pair "latches" in the "ON" state until the DC source for the latch is removed. Removal of this DC source occurs when C1 discharges through CR1, thus removing DC voltage from the control IC. Notice also that the kick start latch, Q4 and Q5, is still in the "ON" state and thus provides a discharge path for C14. When the decreasing voltage across C14 is less than approximately one volt, the Q4-Q5 latch also switches off.

At this point in time, all circuits are in an OFF condition except the input DC supply. C14 now begins to re-charge toward the input DC supply to restart the power supply. If a fault remains, the kick start and current limit circuits will continue to shut-down and re-start the power supply several times per second until the fault is removed or AC power to the supply is turned-off.

Under-Voltage Lockout

The Under-Voltage Lockout, UVL, shuts down the supply whenever the AC input voltage drops below about 9Ø volts. This occurs when the voltage at pin 13, set by the divider action of R27 and R25, diminishes to a level below the internal reference supply of the control IC. Pulses are inhibited immediately and because the DC supply to the Control IC is no longer replenished by the auxiliary supply, it discharges toward zero.

Why is it important to shut down the supply if the input AC line drops below 9Ø volts? The answer will become clear when an inherent characteristic of the circuit is discussed, namely, its negative input resistance.

Imagine the situation where the supply is delivering full power to its load and the AC input voltage drops five or ten volts. The supply control circuit responds by increasing the "ON" time of the switching transistor thus increasing the average current in the primary winding. The only way the DC supply can deliver more current is to draw it from the AC line. So the negative change in AC input voltage was accompanied by a positive change in AC input current.

A-other way to describe this characteristic is that the supply is a constant power device, that is:

$$P_{in} = V_{in} \times I_{in} = \text{constant}.$$

Thus if V decreases, I will increase, and vice versa. The supply will thus draw more and more current from the AC line if the AC voltage continues to decrease. In order to limit the average current to a safe value, the control circuit senses the input voltage and shuts down the supply before the AC voltage level becomes too low or the AC current input becomes too high.

Secondary Outputs

Each of the secondary windings consist of a half-wave rectifier followed by a pi filter. The input capacitor of the filter stores the charge delivered to it when the rectifier is biased ON by the polarity of the transformer winding. The inductor and the output capacitor form a low-pass filter which removes the switching frequency ripple component.

The current output of the -12 volt supply is much smaller than that of the positive voltage outputs. Because of this, the current limit circuit response is not sufficiently effective to prevent damage to the -12 volt circuit. Therefore, a three terminal regulator with its own current limiting circuit is used to protect the -12 volt output.

All of the 12-volt rectifiers are fast recovery types and the +5 volt rectifier is a Schottky type. These diodes feature high switching speeds during turn-off. Their low forward voltage drop mimimizes dissipation resulting in maximum efficiency. Each of the positive outputs has a bleeder resistor.

The reason for two separate +12 volt outputs is to provide sufficient isolation between different types of loads. It is easier to regulate the +12 volts if the load which contains the DC motors in the disk drives is separated from the rest of the loads. In addition, the +12 volt "Disk" output (V3) is included in the load sense network in order to minimize the load transients which occur when the disk drives turn on and off. The supply is then better able to regulate the other +12 volt output (V2) during the severe V3 transitions.

Load Sense and Feedback Signal Development

The circuit of Figure 21 has three parts. In part (a), the IC's U2 and U3 are biased ON by resistors R11 and R22. These resistors also sense the changes in AC line input

voltage to provide line regulation. U2A is the LED half of an optocoupler which serves to isolate the DC ground circuits of primary and secondary while coupling the AC feedback signal via optical coupling. U3 serves as both a stable DC reference voltage which the output voltages are compared against and as an error amplifier which provides the gain necessary for adequate sensitivity of the control IC to load changes.

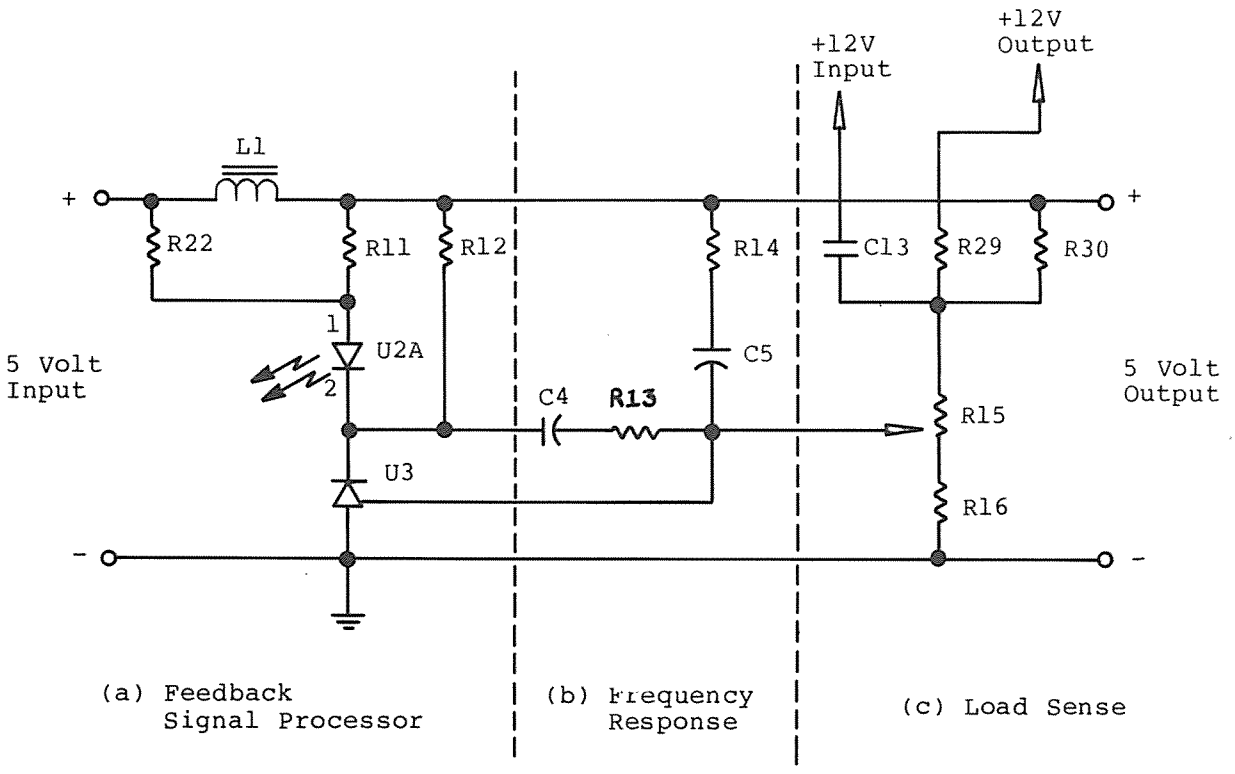


FIGURE 21. FEEDBACK SIGNAL DEVELOPMENT

Each of the passive components in the load sensing network is a high stability (+/- 1ØØppm) part to assure stability of the network over the operating temperature range of the power supply.

Part (b) of Figure 21 includes the network which tailors the frequency response of the error amplifier so that it responds to low frequency change only. This network, consisting of R14/C5 and R13/C4, also determines the stability of the power supply by ensuring that the power supply control circuit has no tendency to oscillate.

Part (c) illustrates the load sensing network. Equal currents through R15 are supplied from the +12V DISK and +5.Ø5V outputs by R29 and R3Ø. In addition, a portion of the transient signal occurring on the +12V CRT output (when the motors turn on or off) is fed to R15 by C17. The wiper of R15 feeds a control signal which represents the status of the current loads to the error amplifier U3. U3 amplifies and compensates it then U2 couples that control signal to U1 where it is used to vary the switching transistor (Q7) ON time to adjust the output voltages as necessary. R15 is adjustable to provide the initial set-up of the +5.Ø5V output when it is installed in a computer.

Overvoltage Crowbar

Some of the circuits supplied by the +5 volt output are quite sensitive to voltages in excess of 7 volts. Since some circuits require both +5 and +12 volts, a failure in those circuits could apply +12 volts to the +5-volt bus and thus damage some of the +5-volt circuits. To prevent the +5-volt bus from exceeding a safe level, an SCR, Q6, is used to "crowbar" or short-circuit the +5.Ø5 volt output to the secondary ground bus. This short circuit triggers the current limiting circuit and the supply shuts down until it trys to restart.

Referring to Figure 22, VR2 sets the turn-on point of the SCR and R17 develops the gate signal when VR2's Zener breakdown voltage of 5.6 volts is exceeded. C6 and R17 provide current limiting for VR2 and filter the gate signal so Q6 won't respond to transient signals.

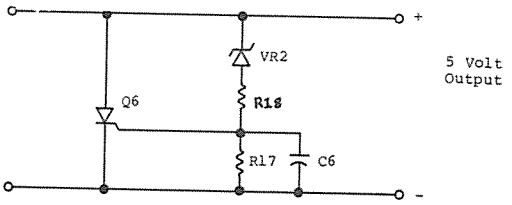


FIGURE 22. OVERVOLTAGE CROWBAR

Power Chain

In a sense we have already analyzed the power chain in the section on basic principle of operation. The base drive causes the switching transistor to turn on and off at a prescibed rate. This action alternately stores energy from the DC input in the primary inductance and releases it into the secondary through the flyback transformer action. The energy is then stored in the input filter capacitor at a voltage determined by the transformer turns ratio. Notice that the turns ratio determines the ratio of collector voltage to secondary voltage, both of which are alternating voltages. The ratio of input-to-output DC voltage is determined by the duty cycle and the turns ratio together.

For example, lets look at the +5 volt output of Figure 23 at normal loading and approximately 12Ø VAC input. Under these conditions, the DC input voltage is 168 VDC and the duty cycle is approximately 4Ø%. Thus, our average DC voltage at the switching transistor collector (or across the primary) is 4Ø% of 168 or 67.5 volts. Dividing this average DC

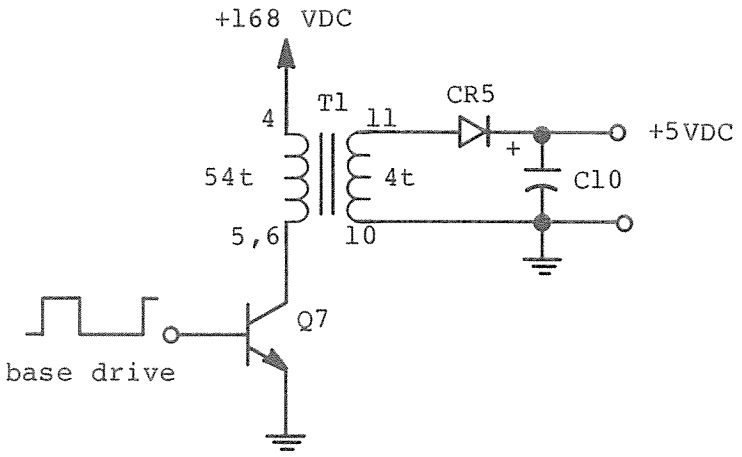


FIGURE 23. POWER CHAIN

voltage by the turns ratio for the 5 volt secondary (54 : 4 = 13.5) gives us 5.Ø volts.

$$\frac{67.5V}{13.5} = 5V$$

Control Chain

Imagine the load end of the feedback path disconnected from the +5.Ø5 volt output terminal and unfolded so that the load sense network is now at the "input". The secondary rectifier (CR5) and filter (ClØ-Cl2, Ll,) remain as the output. The circuit as it now appears, redrawn in simplified form in Figure 24, is known as the control chain. To see how the regulation action occurs, assume a small negative voltage change at the "input" of the feedback network and follow it through the control chain.

This negative voltage change, which would correspond to a slightly heavier load current, appears at pin 1 of U3 as a decreasing voltage. The error amplifier in U3 inverts and amplifies this signal. The positive-going output voltage of U3 at pin 3 causes less current to flow in the internal LED of U2A. A replica of this smaller current, optically coupled and induced in the phototransistor of U2B, develops a reduced voltage across R7 at the non-inverting input of the regulator error amplifier in Ul.

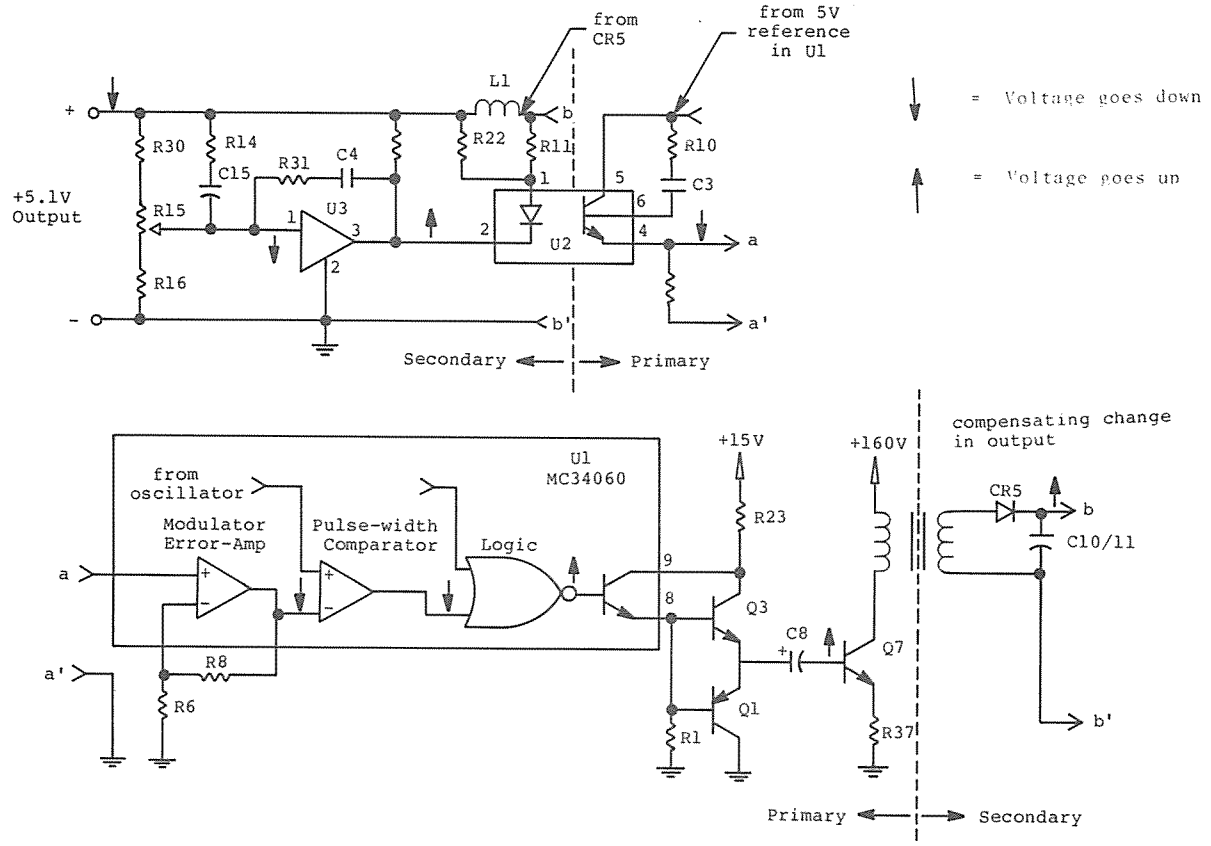


FIGURE 24. CONTROL CHAIN SIMPLIFIED SCHEMATIC

The regulator error amplifier in U1 does not invert the signal, but further amplifies it, improving the sensitivity of the control chain to small changes at the power supply output. The regulator error amplifier output is Vreg. Since we established earlier that a negative-going Vreg increases the length of the base drive pulse, Q7 is turned on a little sooner so that it can store more energy from the AC line in the primary inductance. Finally, this increased energy is stored in the filter capacitor C1Ø,C11 during the flyback interval and supplies the increased demand for current that resulted in the original reduction in the output voltage.

More simply stated, the control chain uses an amplified version of the output voltage CHANGE to adjust the width of the base drive pulse through the action of a control voltage at a comparator input.

Troubleshooting Chart

Trouble	Cause	Remedy
open fuse	shorted line input filter capacitor	check and/or replace C33, C32, C31, C3Ø
	shorted bridge	check BR1
	shorted filter capacitor	check C29, C26, R39
	shorted switching transistor	check Q7, C37, R4Ø, C26, T1 pri., Q3, Q1, R37
Current limit cycle	single rectifier open in bridge	check and/or replace BR1
	open filter capacitor	check C29
	shorted snubber capacitor or resistor	check C37, R4Ø
	open opto-coupler	check U2
	shorted supply output	check computer for short on +5V, +12V CRT, +12V DISK, -12V outputs and clear shorted condition
	shorted output rectifier	check CR5, CR6, CR7, CR8
	open or shorted output filter capacitor	check C16, C18, C25, C23, C1Ø, C11, C12, C19, C2Ø
	defective crowbar	check Q6

Troubleshooting Chart (cont'd)

Trouble	Cause	Remedy
no pulses at pin 8 of U1, (i.e., supply shut down)	no aux. DC supply	Check and/or replace CR4, C14, T1 aux.
	no "kick start"	check R26, Q4, Q5, VR1, CR1, C1
	no base drive	check U1, Q3, R23, C8, R24
	dead-time control divider malfunction	check C2, R4, R5, U1 (for V ref.)
	under-voltage protect divider malfunction	check R27, R25, C9, Q9
	PWM feedback malfunction	check and/or replace U1, U2, C3

Testing and Adjustments

The following tests should be performed to guarantee correct operation of the power supply after repairs have been made. The first test checks the primary circuits and is to be made without AC power applied. The second test is a complete operational test with AC power applied.

Primary, Checks T2, U1

No AC Power Applied

1. Apply +35 volts DC via 17Ø ohm, 5 watt resistor from Q4 emitter to the primary side of ground. Primary side ground is the point labeled ▽ on the schematic. Also apply 35 volts DC via a 12Øk ohm resistor and a normally closed SPST switch from Pin 13 of U1 to primary ground. Observe the voltage across C14 as it charges. As it reaches a value near +31 volts, it should drop to near +16 volts as Q5 and U1 turn on.

2. Check U1 pin 8 and/or Q7 base for a base drive pulse: a 4Ø kHz square wave of 8/4 volts respectively

3. Switch the SPST switch connecting the 12Øk ohm resistor from Pin 13 of U1 and check for loss of base drive pulses on Q7.

Operational, Checks T2, U1, U2

Apply AC Power

1. Apply rated maximum loading for condition 1 (Model III use) or condition 2 (5 1/4" Hard Disk use).

2. Apply 12Ø VAC input voltage and observe Q7 current (via loop on PCB) and voltage (at TP2). Supply should start in two to four seconds.

3. Observe the +5.Ø5 volt output and adjust R15 until the output is exactly +5.Ø5 volts DC.

4. Measure +12V and -12V outputs.

5. Check all outputs at Vin = 9Ø VAC and 135 VAC at:
   (a) minimum and maximum loads
   (b) check +12V CRT when +12V DISK varies in transient test.

6. Measure ripple. See Measurement Techniques below.

7. Measure efficiency. See Measurement Techniques below.

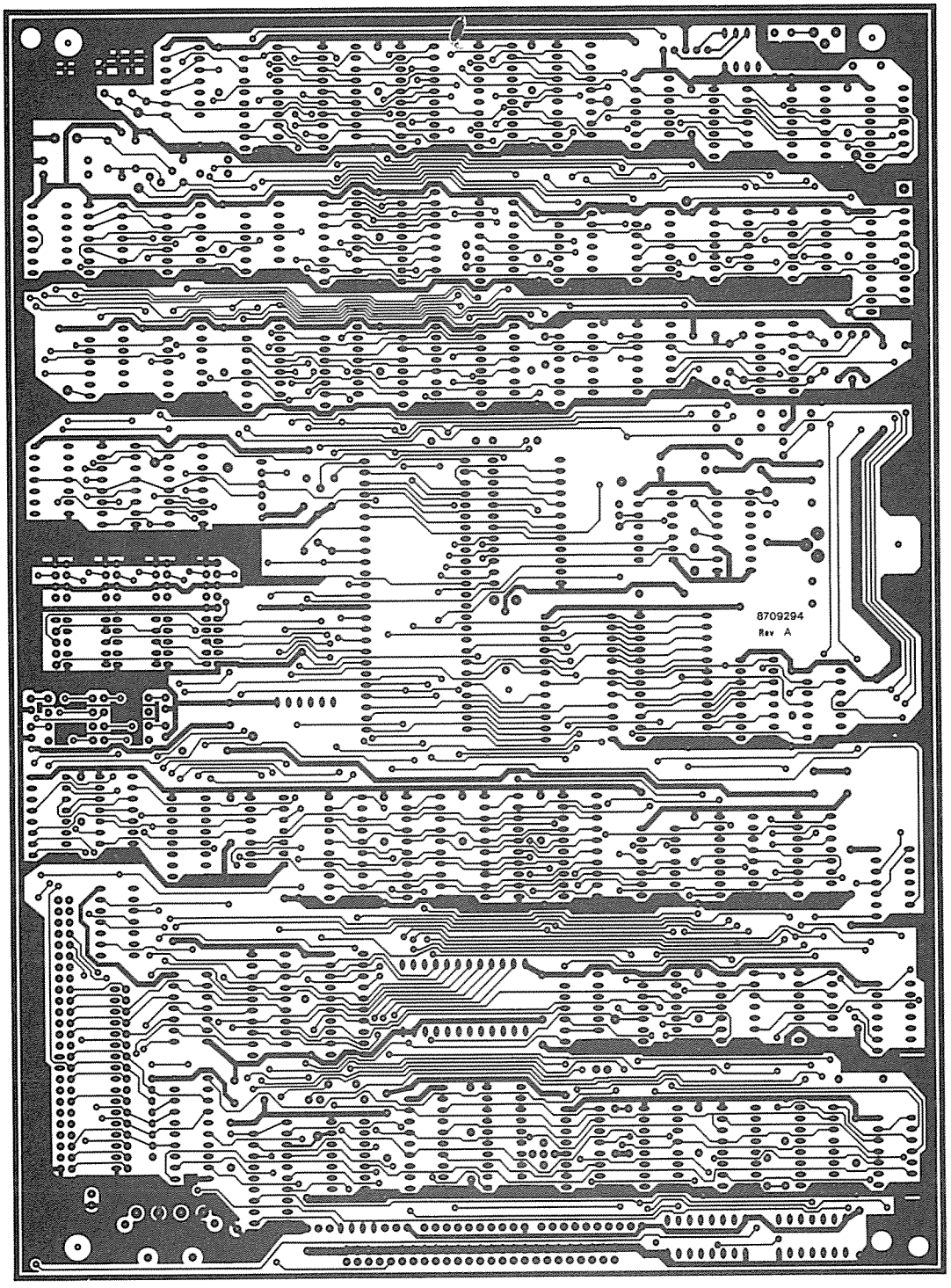
8. Test operation of current limit and over-voltage protection circuits by applying +7.Ø volts to the +5 volt output.

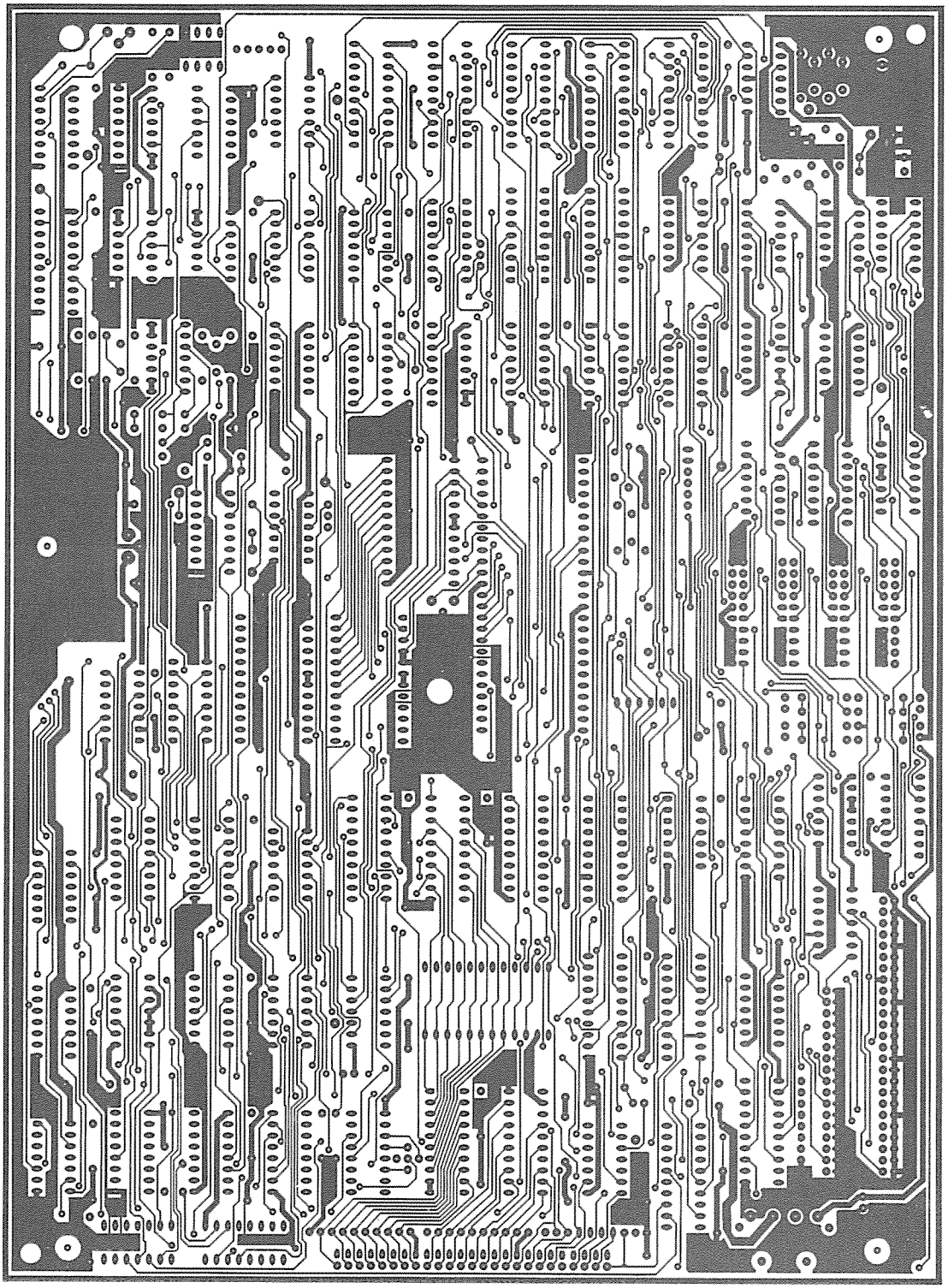
Measurement Techniques

1. Ripple -- Unit connected to full load at low line. One end of 5Ø ohm coaxial cable connected to output terminals. Other end of cable (terminated with Ø.ØluF ceramic cap in series with 51 ohm resistor) connected to scope using BNC T-fitting. Two components at 12Ø Hz and 4Ø kHz.

2. Efficiency -- Use Diego Systems Series 2ØØ power monitor. Efficiency = $\frac{\text{Power Out}}{\text{Power In}}$

10/ Printed Circuit Boards

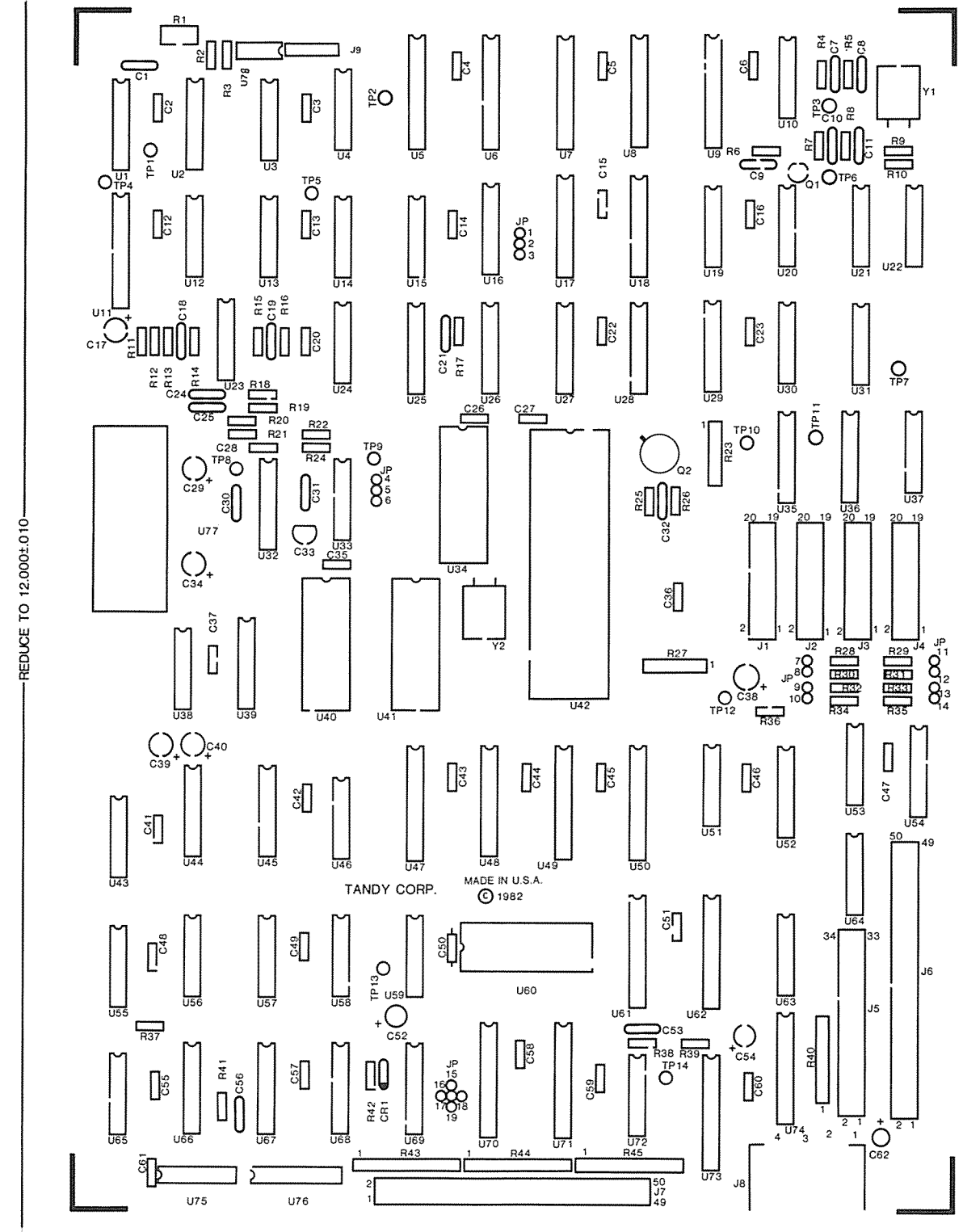




REDUCE TO 12.000±.005

REDUCE TO 9.000±.005

TANDY CORP. COMPONENT SIDE 1700189 REV A CONTROLLER BOARD


REDUCE TO 12.000±.010
REDUCE TO 9.000±.010
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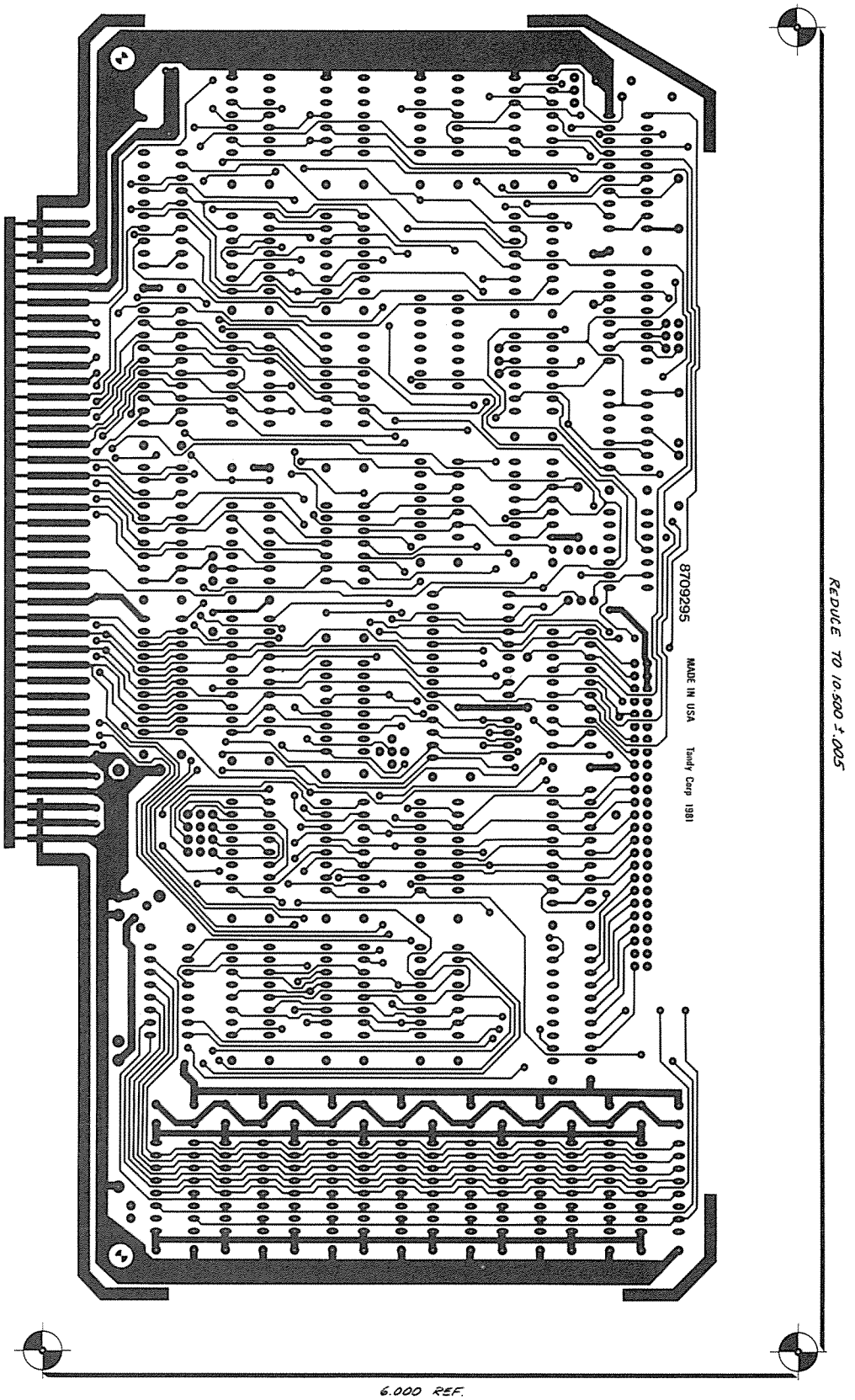
REV "A"
CONTROLLER BOARD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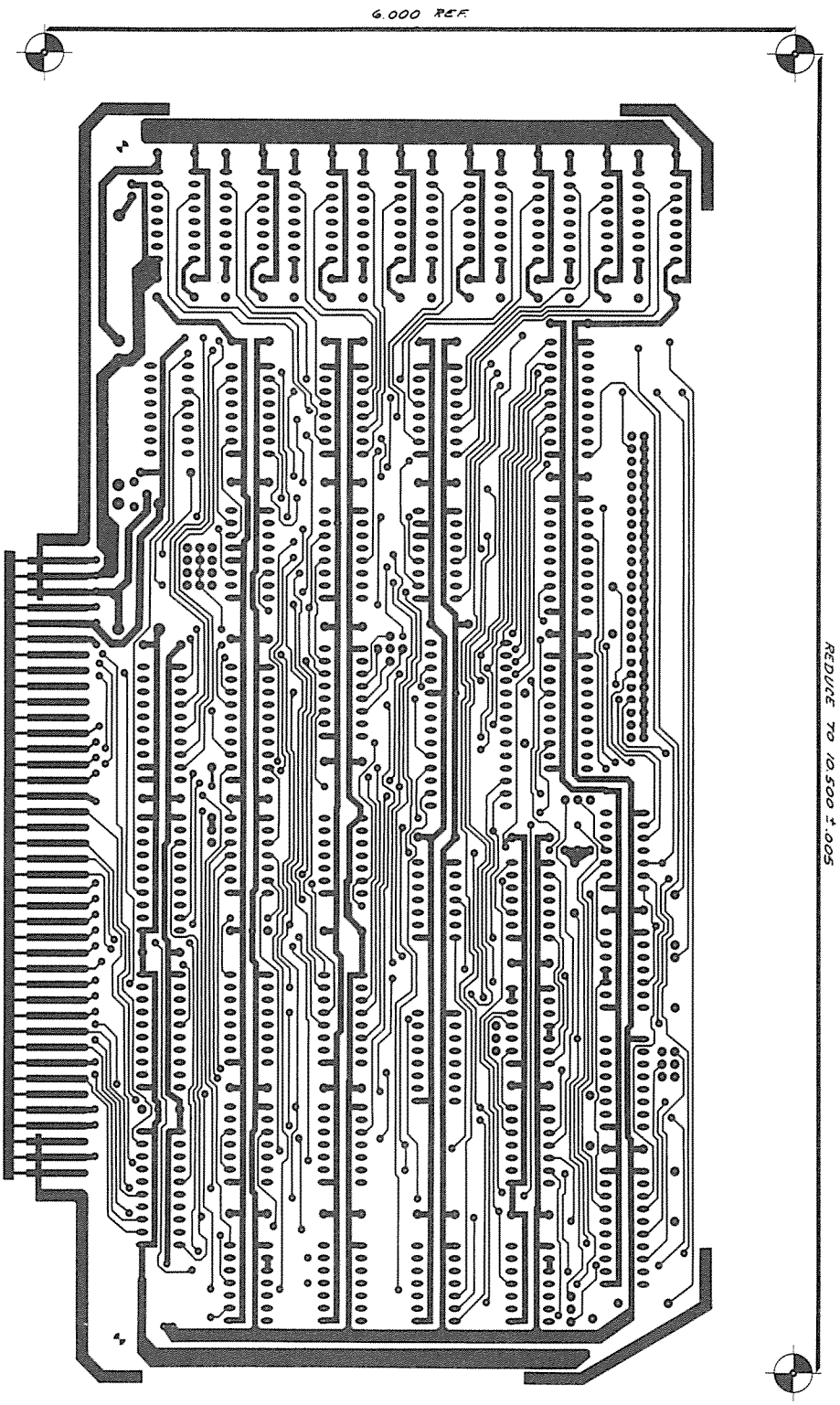
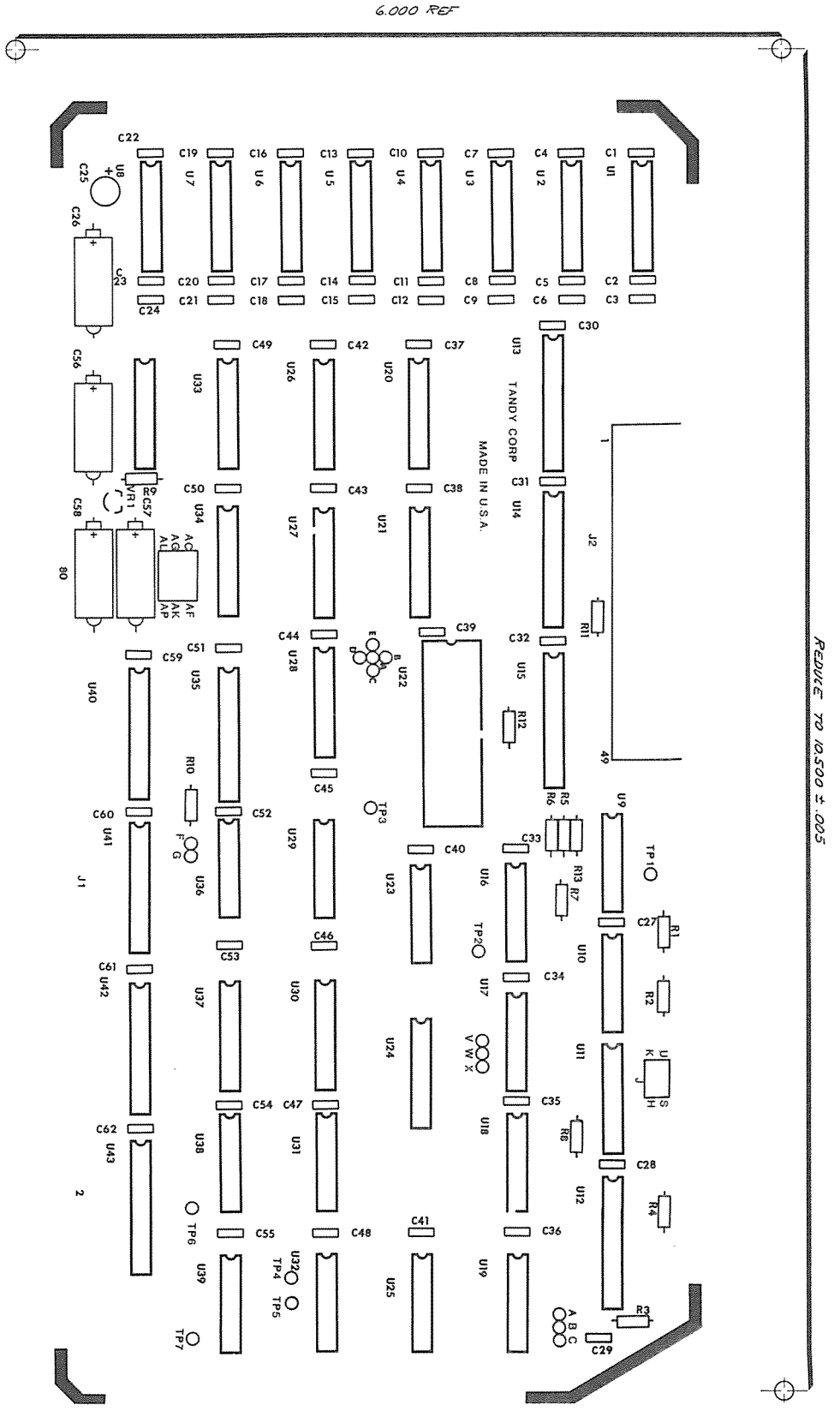
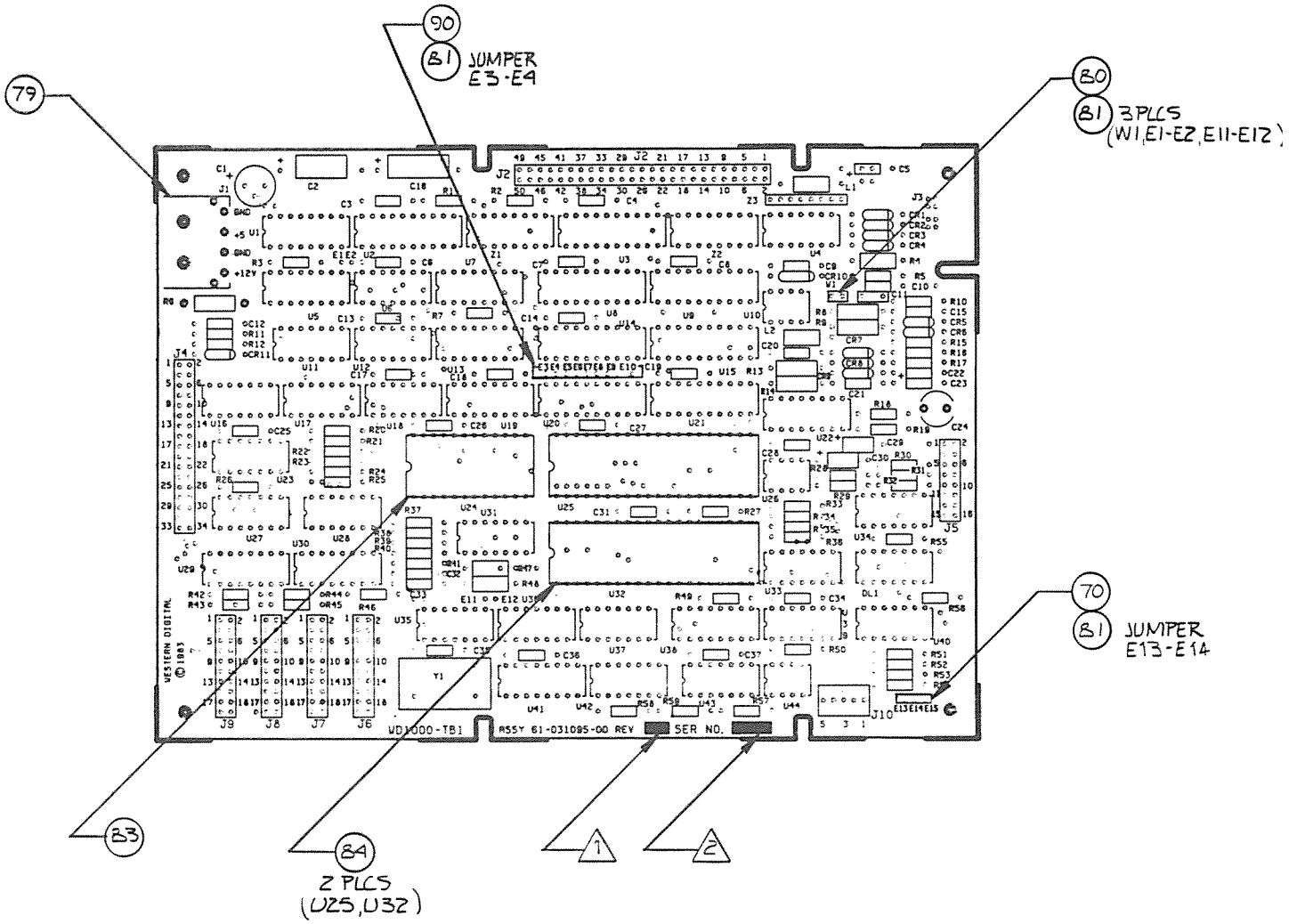
Tandy Corp 1981
REDUCE TO 10.500 ±.005
6.000 REF.


6.000 REF.
REDUCE TO 10.500 ±.005


6.000 REF
TANDY CORP
MADE IN U.S.A.
REDUCE TO 10.500 ± .005
J1
J2



REV	ECO	DESCRIPTION	BY	CK	APPR	DATE
X3	681	REV LEVEL CHANGE ONLY			ARF	11-22-83
X2	654	ADDED JUMPER E13-E14	PJD		ARF	11-9-83
X1	622	REV LTR CHANGE ONLY			ARF	10/11/83
X0	610	PROTOTYPE RELEASE	SF		SRL	9-29-83

TOLERANCES EXCEPT AS NOTED: PLACES XX ± 010, XXX ± 005; ANGLES ±0°30'; HOLES +.004 -.001; DO NOT SCALE DWG.

	SIGNATURE	DATE
DRAWN	P.J. DIAZ	9-21-83
CHECK		
ENGINEER	NADER SHAU	
ENGR APPR		
Q A APPR		
MFG APPR		

WESTERN DIGITAL CORPORATION

TITLE: WD-1000-TB1 ASSEMBLY

CLASS CODE	BASE NUMBER	DASH	BIN/ROM CODE	REV	DCLC
61	031095	0010	—	X3	—

SCALE 1/1 SHT 1 OF 1

A

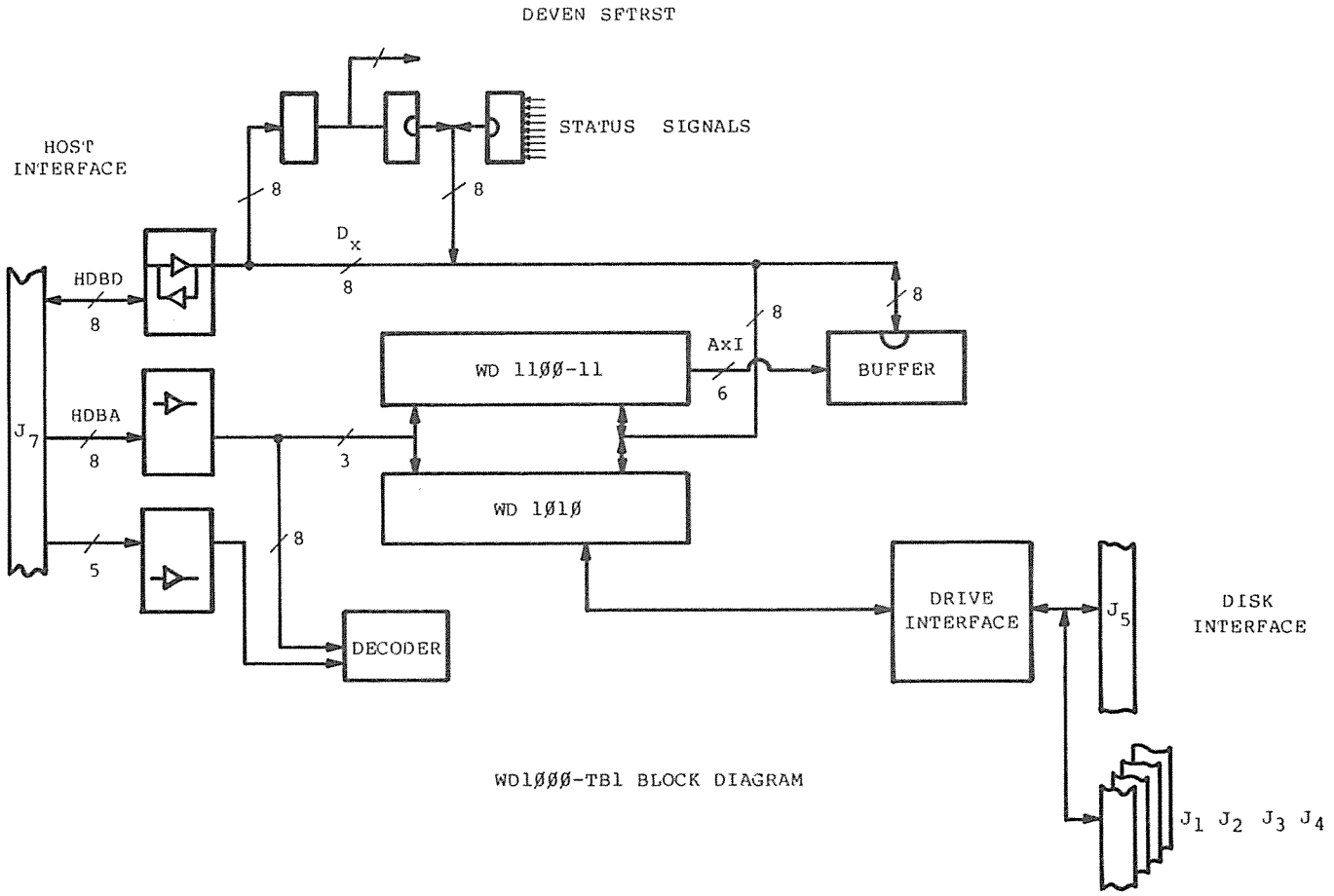
3. REF. DOCUMENTS: BILL OF MATERIAL 61-031095-0002
SCHEMATIC 61-031095-0011

4. STAMP APPROPRIATE SERIAL NUMBER IN AREA SHOWN

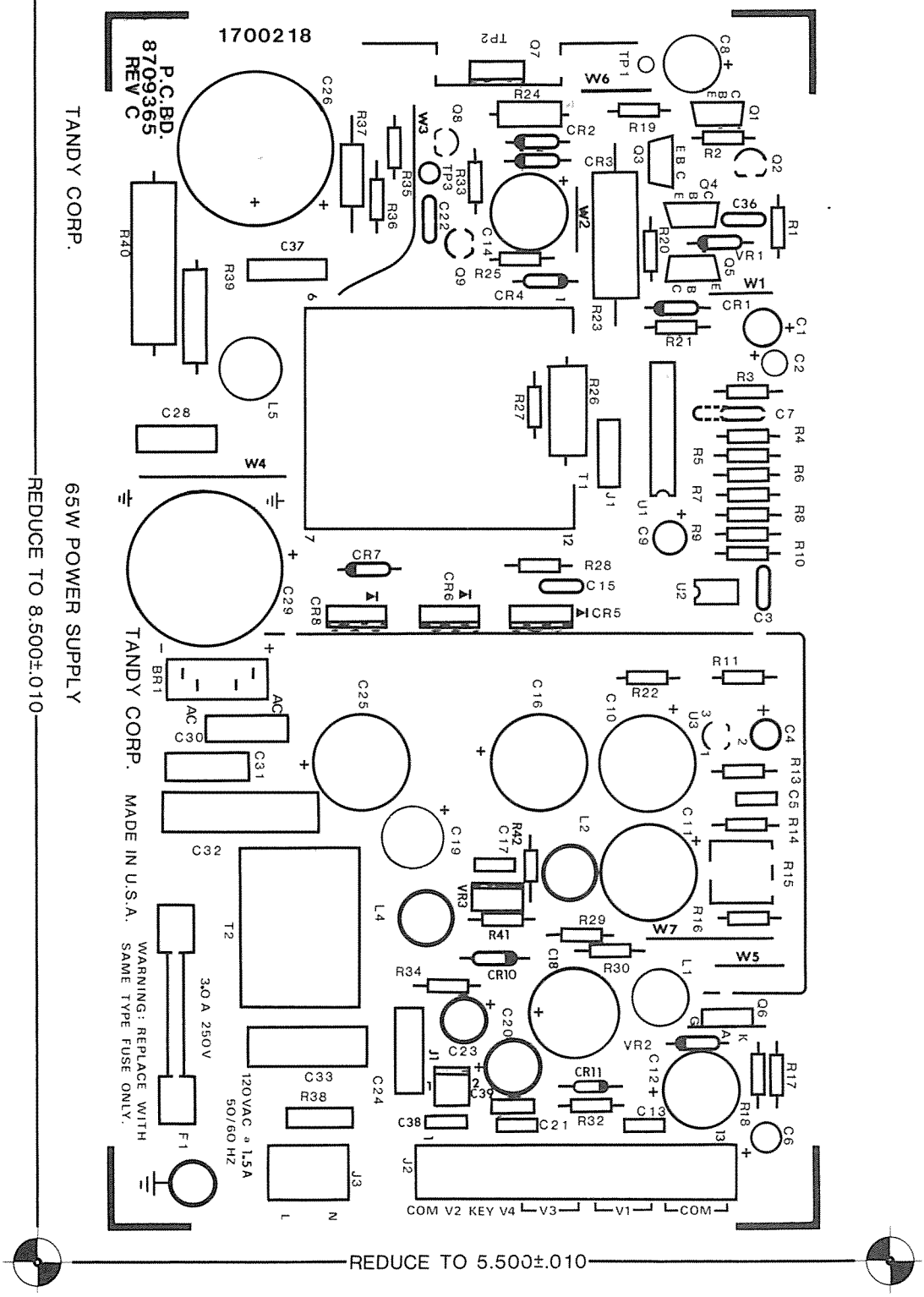
5. STAMP APPROPRIATE REVISION IN AREA SHOWN

NOTES:

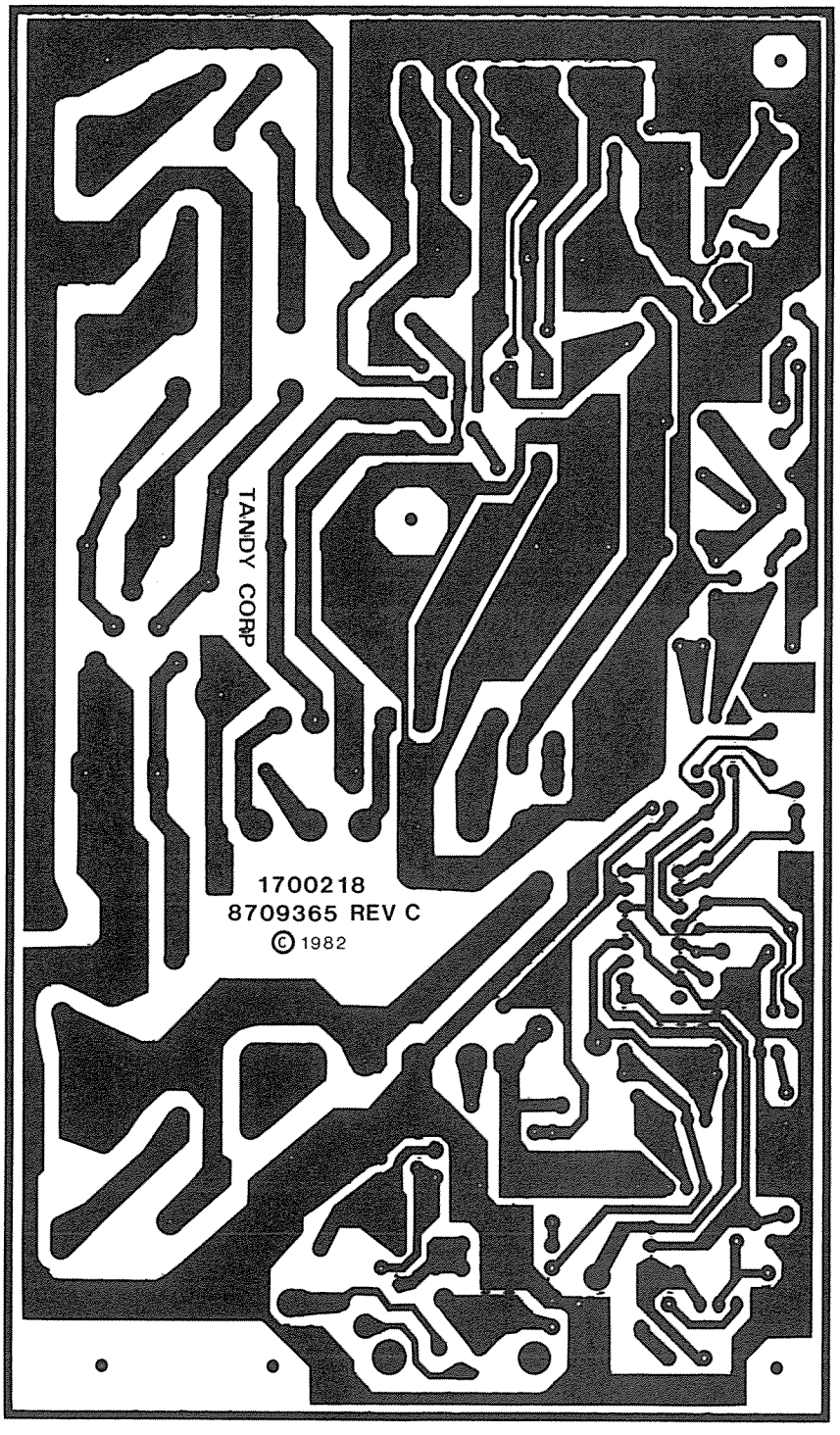
1



WD1ØØØ-TB1 BLOCK DIAGRAM


1700218
P.C.BD.
8709365
REV C
TANDY CORP.
65W POWER SUPPLY
REDUCE TO 8.500±.010
TANDY CORP. MADE IN U.S.A.
WARNING: REPLACE WITH SAME TYPE FUSE ONLY.
3.0 A 250V
120 VAC @ 1.5A
50/60 HZ
COM V2 KEY V4 V3 V1 COM
REDUCE TO 5.500±.010

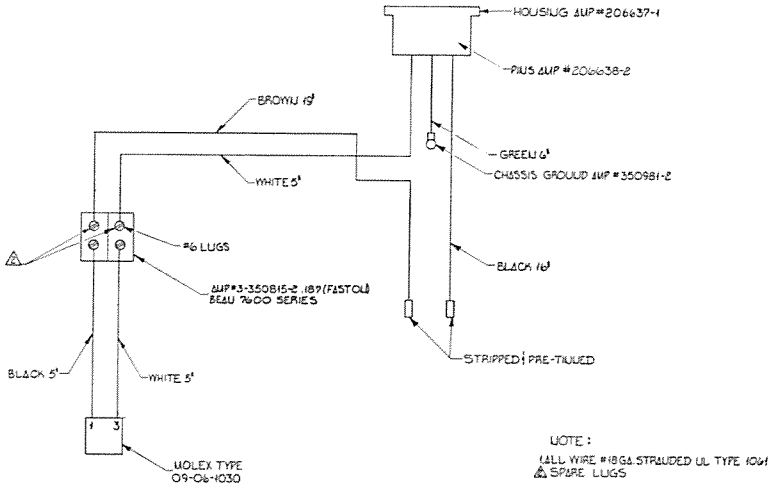
REDUCE TO 5.500±.005



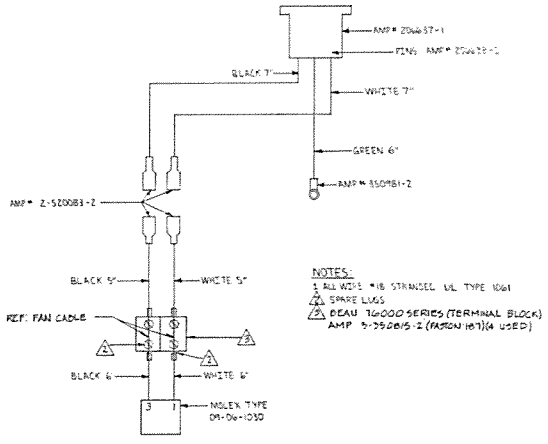
TANDY CORP. 65W POWER SUPPLY

REDUCE TO 8.500±.005

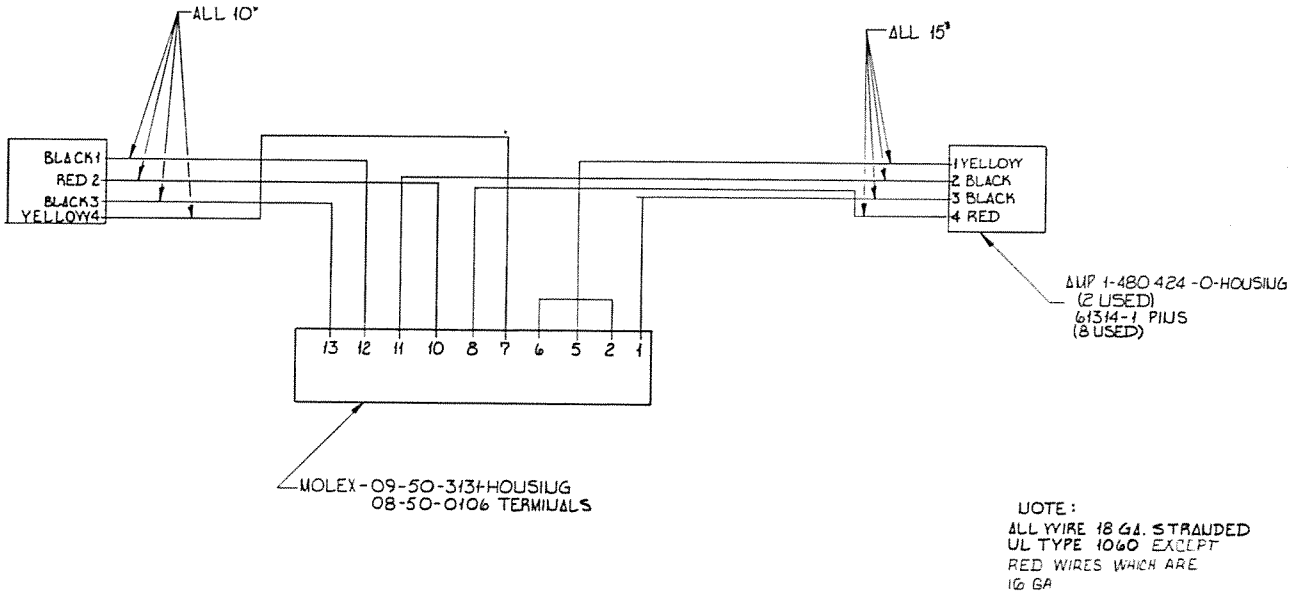
11/ Wiring Diagrams



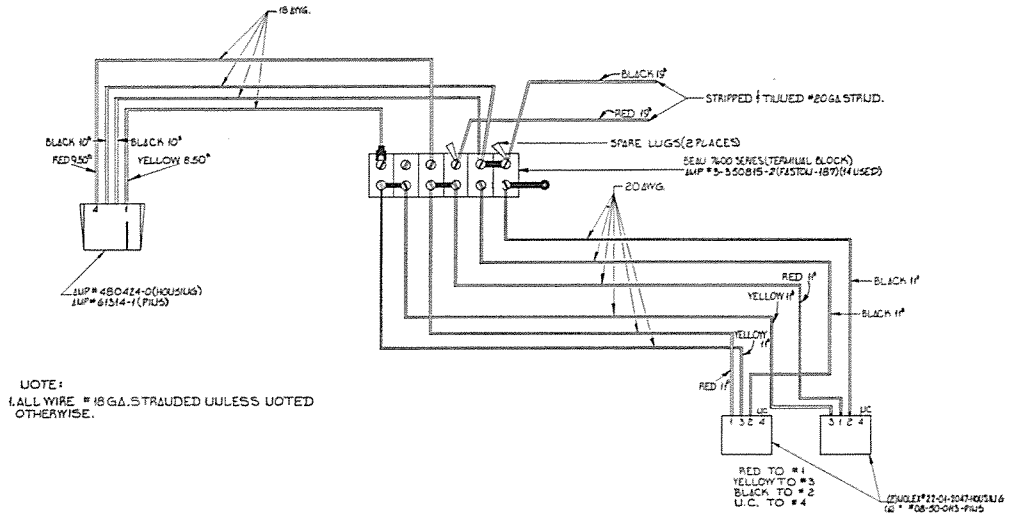
AC Wiring Harness (Primary/Master)



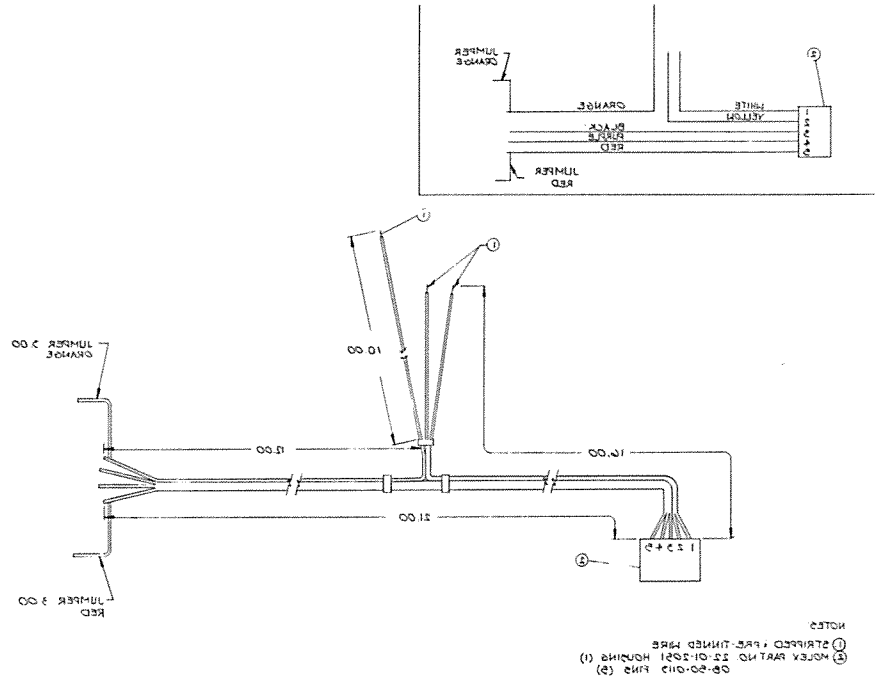
AC Wiring Harness (Secondary/Slave)



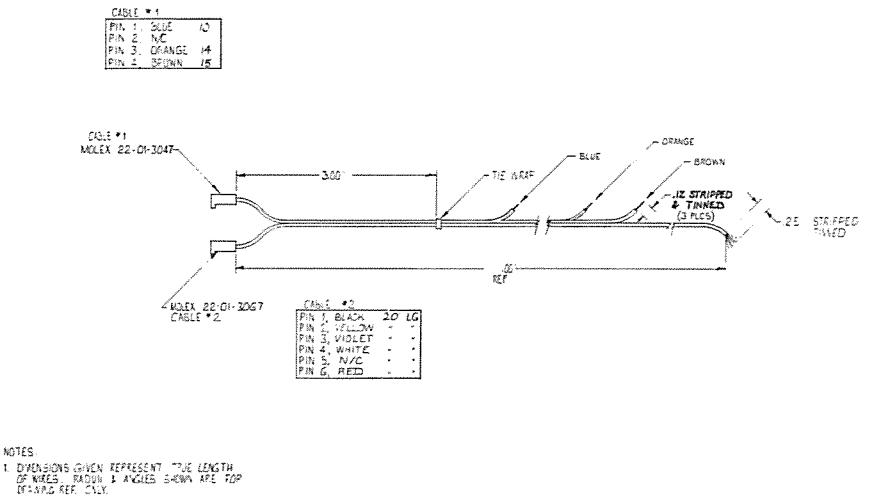
DC Power Harness (Primary/Master)



DC Power Harness (Secondary/Slave)

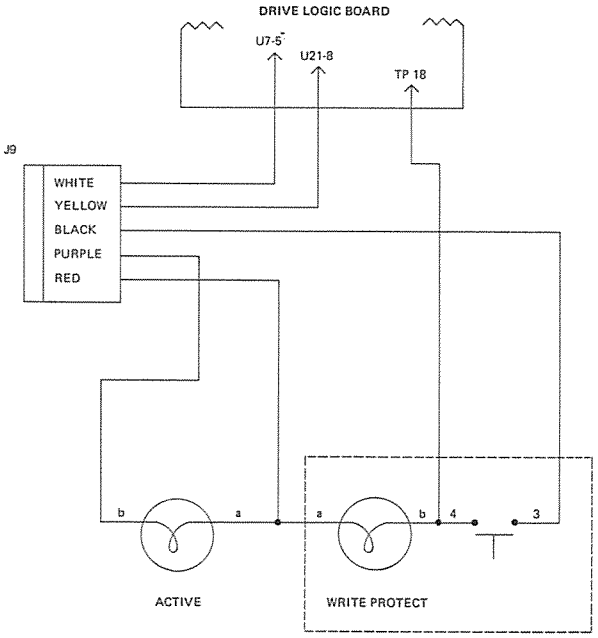


Lamp Driver Wiring Harness (Primary)



NOTES:
1. DIMENSIONS GIVEN REPRESENT TRUE LENGTH OF WIRES. RADIUS & ANGLES SHOWN ARE FOR DRAWING REF. ONLY.

LED Driver Board Harness (Secondary)



Standard Jumpers on Controller Board

17 - 19 1 - 2 5 - 6

12/ Parts Lists

PRODUCT DESCRIPTION
HARD DISK 5 1/4"
CAT. NO. 26-4152

QTY	DESCRIPTION	PART NUMBER
1	MANUAL, START-UP	8749389
1	REFERENCE, MANUAL	8749394
1	MANUAL ASSY	8898419
1	LABEL, TOP H.D. CONN	8789613
1	CORD, 8' POWER*	87Ø9Ø57
1	CABLE, EXT	87Ø9244
1	KIT, ACCESSORY HDM	8898418
1	CASE, BOTTOM*	8729124
1	PLUG, 2 1/2" DIA.	8729148
1	LABEL, FCC PART 15	8789287
1	LABEL, FCC ID HDM	8789Ø8
1	LABEL, S/N	878979Ø
4	FOOT	859Ø123
4	WASHER, 1/2 O.D	8589Ø74
4	SCREW, #1Ø X 1/2"*	8569Ø62
3	PLATE, COVER	8729147
6	SCREW, #4X1/4 PPH	856912Ø
1	CABLE, INT. CNTRL	87Ø933Ø
1	CABLE, INT.CNTRLR	87Ø9331
2	SCREW, #6 X 5/16	856913Ø
2	SCREW, #4-4Ø X 3/4"PPH	8569Ø59
2	NUT, LOCK #4-4Ø	8579ØØ3
2	WASHER, STAR #4	8589Ø75

1	HARNESS, AC MSTR	87Ø9332
1	SCREW, #6-32 X 1/4 (GRD)	8569Ø98
2	SCREW, #4-4Ø X 1/2"PPH	8569Ø33
2	NUT, LOCK #4-4Ø	8579ØØ3
1	FAN, COOLING*	879Ø4Ø1
2	TAB, FASTON	8529ØØ8
4	NUT,#6-32 KEPS	8579ØØ4
1	FAN, 5M S/A	889662Ø
1	BEZEL, SWITCH*	871923Ø
1	SWITCH, KEYLOCK*	8489Ø47
1	SWITCH, ON/OFF*	8489Ø48
1	INDICATOR LIGHT*	8469ØØ9
1	BEZEL ASSY	889661Ø
1	DRIVE, 12 MEG HARD	879Ø2Ø3
4	METAL SLEEVE	8589Ø76
1	HARNESS, LAMP	87Ø9347
2	MOUNT, DRIVE	8729179
4	WASHER, LOCK #6	8589Ø18
4	SCREW, #6-32 X 1/4 PPH	8569Ø98
4	GROMMET, RUBBER	859Ø127
1	DRIVE, S/A	8896Ø9
1	FILTER	8719298
4	NUT,LOCK #6-32	8579ØØ4
4	SCREW, #6-32 X 2 F.CNTSK	8569155
2	SCREW, #6-32 X 1/2	8569126
2	SCREW, #6-32 X 1/4 THD FM	8569Ø4Ø
4	SCREW #6-32 X 1/4"PPH	8569Ø98
4	WASHER, #6	8589Ø18
1	CLIP, CORD .52" DIA.	8559Ø15
1	CLIP, CORD .38" DIA.	8559Ø1Ø
7	TUBING 1/8DX1/2	8539Ø25
1	PCB ASSY, CONTROLLER* (See pages 71-74)	889613Ø
2	IC P2114 U17, U18	8Ø42114
1	IC, 8X3ØØ MICRO-CONT	8Ø4Ø3ØØ
1	IC 28S86 BPROM (U34)PRGMD	8896Ø3
1	IC, 28S86 BPROM (U4Ø)PRGMD	8896Ø2
1	IC, 28S86 BPROM (U41)PRGMD	8896Ø4

1	IC, WD 11ØØ-Ø1 (U9)	8Ø4Ø111
1	IC, WD 11ØØ-12 (U5)	8Ø41112
1	IC, WD 11ØØ-Ø3 (U11)	8Ø4Ø113
1	IC, WD 11ØØ-Ø4 (U6)	8Ø4Ø114
1	IC, WD 11ØØ-Ø5 (U7)	8Ø4Ø115
1	PCB, CONTROLLER 5M F/A	8896ØØ
1	POWER SUPPLY*	8729189
1	INSULATOR	8539Ø26
1	POWER, SUPPLY	879ØØ43
4	SCREW, #6-32 X 1/4"PPH	856916Ø
4	WASHER, #6 LOCK	8589Ø18
2	SCREW, #1Ø X 1/4"PH	8569153
1	WASHER, .141 1DX .167 OD	8589Ø72
5	SCREW, #6-32X3/8"PPH	8569ØØ3
1	POWER SUPPLY S/A	8896Ø8
1	HARNESS DC MSTR	87Ø9334
4	SCREW, #6-32X1/4 PPH	856916Ø
4	WASHER, #6 LOCK	8589Ø18
1	HOLDER, PLASTIC MAP	859Ø1Ø9
1	CABLE, INT. DATA MSTR	87Ø9324
1	COVER, TOP	8729123
2	CLIP, GRD.	8559Ø4Ø
5	SCREW, #8-32X3/8"	8569107
5	WASHER, #8 FLAT	8589Ø27
1	LOGO STRIP*	8719221
1	BEZEL*	8719209
1	COVER, TOP S/A	8898Ø3
3	SCREW, #6-32X3/8" PPH	8569Ø26
1	LABEL, LINE TERMINATOR	8789597
1	MANUAL, SERVICE	8749Ø3
1	PCB ASSEMBLY, INTERFACE (See pages 75 and 76)	8898417

PRODUCT DESCRIPTION
5 1/4" HARD DISK
CAT. NO. 26-4153

QTY	DESCRIPTION	PART NUMBER
1	CABLE, EXT. DATA 2ØPOS.	87Ø9384
1	CABLE, EXT. CNTRL 34POS.	87Ø9329
1	CORD, 8' POWER*	87Ø9Ø57
1	CABLE, INT. DATA 2Ø POS	87Ø9326
1	KIT, ACCESSORY HDS	8898ØØ7
1	CASE BOTTOM*	8729181
1	LABEL, FCC PART 15	8789287
1	LABEL, FCC ID HDS	8789809
4	FOOT	859Ø123
4	SCREW, #1Ø X 1/2"	8569Ø62
4	WASHER, 1/2 O.D.	8589Ø74
1	LABEL, S/N	8789793
1	CABLE, INT CNTRLR	87Ø9325
1	CABLE, INT. CNTRL/SLV	87Ø9328
2	SCREW, #6 X 5/16 BRICO IND.	8569139
2	SCREW, #4-4ØX3/4 PPH	8569Ø59
2	NUT,#4-4Ø KEPS LOCK	8579ØØ3

2	WASHER, #4 STAR	8589Ø75
1	FAN, COOLING	879Ø4Ø1
2	TAB, FASTON	8529ØØ8
1	FAN, 12M S/A	889662Ø
4	SCREW, #6-32 X 2" FCNTR	8569155
1	FILTER	8739Ø1Ø
4	NUT, #6-32 LOCK*	8579ØØ4
1	HARNESS, AC SLV	87Ø9333
2	SCREW, #4-4Ø X 1/2"PPH	8569Ø33
2	NUT, LOCK #4-4Ø	8579ØØ3
1	BEZEL, SWITCH*	871923Ø
1	INDICATOR, PWR ON	8469Ø11
1	SWITCH, ON/OFF*	8489Ø48
1	INDICATOR LIGHT*	8469ØØ9
1	BEZEL ASSY	8896611
1	HARNESS DC ASSY	87Ø9335
1	RELAY, 12V 7ØMA	8429Ø4
4	SCREW, #6-32 X 1/2	8569126
2	SCREW, #6-32 X 1/4	8569Ø98
2	SCREW, #6-32 X 1/2	8569152
2	SCREW, #6-32 X 3/8	8569Ø26
2	CLIP CORD .38 DIA.	8559Ø1Ø
7	TUBING 1/8 DIA. X 1/2	8539Ø25
1	DRIVE, 12 MEG HARD	879Ø2Ø3
1	HARNESS, LED DRIVER	87Ø9348
1	HARNESS, RELAY	87Ø9355
2	MOUNT, DRIVE	8729179
4	SCREW, #6-32 X 1/4 PPH	8569ØØ3
1	DRIVE, 12M HDS S/A	8898422
1	POWER SUPPLY	879ØØ25
9	SCREW. #6-32 X 1/4 PPH	856916Ø
1	SCREW, #6-32X1 PPH ZINC	8569159
2	NUT, #6-32 KEPS	8579ØØ4
1	PCB DRIVER F/A 12M	8896615

1	HOLDER, PLASTIC MAP	859Ø1Ø9
1	COVER, TOP	8729123
2	CLIP, GRD.	8559Ø4Ø
3	SCREW, #6-32 X 3/8 PPH	8569Ø26
5	SCREW, #8-32 X 3/8	8569Ø17
5	WASHER, #8 FLAT	8589Ø27
1	LOGO, STRIP	8719259
1	BEZEL	8719ØØ9
1	LABEL, WARRANTY NOT.	8789Ø9Ø
1	BAG, 6X15X22	859Ø124
1	LABEL, LINE TERMINATOR	8789597

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(889613Ø)
REV. Ø9/Ø7/82 PAGE 1 OF 4

SYMBOL	QTY	DESCRIPTION	PART NO.
	1	PCB LOGIC BOARD REV. " - "	87Ø9294
TP1-14	14	STAKING PINS	8529Ø14
C1	1	CAPACITOR 68 PFD 5ØV C. DISK	83ØØ683
C2-6	5	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C7-9	3	CAPACITOR 1ØØ PFD 5ØV C. DISK	83Ø11Ø4
C1Ø	1	CAPACITOR 68 PFD 5ØV C. DISK	83ØØ683
C11	1	CAPACITOR 22 PFD 5ØV C. DISK	83ØØ224
C12-16	5	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C17	1	CAPACITOR 1ØØ MFD 16V ELEC. RAD.	8327ØØ1
C18,19	2	CAPACITOR 1Ø PFD 5ØV C. DISK	83ØØ1Ø4
C2Ø	1	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C21	1	CAPACITOR 68 PFD 5ØV C. DISK	83ØØ683
C22,23	2	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C24	1	CAPACITOR .ØØ68 MFD 5ØV POLY	83Ø2684
C25	1	CAPACITOR 15Ø PFD 5ØV C. DISK	83Ø1153
C26-28	3	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C29	1	CAPACITOR 1Ø MFD 16V ELEC. RAD.	8326ØØ1
C3Ø	1	CAPACITOR 33Ø PFD 5ØV C. DISK	83Ø1332
C32	1	CAPACITOR 1ØØ PFD 5ØV C. DISK	83Ø11Ø4
C33	1	CAPACITOR 6-5Ø PF TRIM NPO	836Ø55Ø
C34	1	CAPACITOR .47 MFD 16V ELEC. RAD.	8324471
C35-37	3	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C41-51	11	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C52	1	CAPACITOR 2.2 MFD 25V ELEC. RAD.	8325221
C53	1	CAPACITOR 1ØØ PFD 5ØV C. DISK	83Ø11Ø4
C54	1	CAPACITOR 1ØØ MFD 16V ELEC. RAD.	8327ØØ1
C55	1	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C56	1	CAPACITOR .Ø1 MFD 5ØV C. DISK	83Ø31Ø4
C57-61	5	CAPACITOR .1 MFD 5ØV MONO	8374ØØ4
C62	1	CAPACITOR 47 MFD 16V ELEC. RAD.	8326471
CR1	1	DIODE IN4148	815Ø148
J1-4	4	CONNECTOR 2Ø-PIN HEADER (SIP)	8519121
J5	1	CONNECTOR 34-PIN HEADER (SIP)	851912Ø
J7	1	CONNECTOR 5Ø-PIN HEADER (SIP)	8519117
J8	1	CONNECTOR 4-PIN RIGHT ANGLE (POWER)	8519141
J9	1	CONNECTOR 5-PIN HEADER (SIP) STRAIGHT	8519145
JP1-6	6	JUMPERS	8529Ø14
JP15-19	5	JUMPERS	8529Ø14
Q1	1	TRANSISTOR MPS29Ø7	81ØØ9Ø7
Q2	1	INSULATOR, TRANSISTOR	8
Q2	1	TRANSISTOR 2N532Ø	811Ø32Ø

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(889613Ø)
REV. Ø9/Ø7/82 PAGE 2 OF 4

SYMBOL	QTY	DESCRIPTION	PART NO.
R1	1	TRIM POT 1ØK OHM MULTITURN	8279311
R2,3	2	RESISTOR 2K OHM 1/4 WATT 5%	82Ø722Ø
R4-6	3	RESISTOR 56Ø OHM 1/4 WATT 5%	82Ø7156
R7	1	RESISTOR 27Ø OHM 1/4 WATT 5%	82Ø7127
R8	1	RESISTOR 51Ø OHM 1/4 WATT 5%	82Ø7151
R9,1Ø	1	RESISTOR 27K OHM 1/4 WATT 5%	82Ø7327
R11,12	2	RESISTOR 1ØØ OHM 1/4 WATT 5%	82Ø711Ø
R13	1	RESISTOR 27Ø OHM 1/4 WATT 5%	82Ø7127
R14,15	2	RESISTOR 62Ø OHM 1/4 WATT 5%	82Ø7162
R16	1	RESISTOR 2K OHM 1/4 WATT 5%	82Ø722Ø
R17	1	RESISTOR 43K OHM 1/4 WATT 5%	82Ø7343
R18,19	2	RESISTOR 1ØØ OHM 1/4 WATT 5%	82Ø711Ø
R2Ø	1	RESISTOR 33Ø OHM 1/4 WATT 5%	82Ø7133
R21	1	RESISTOR 68Ø OHM 1/4 WATT 5%	82Ø7168
R22	1	RESISTOR 5.6K OHM 1/4 WATT 5%	82Ø7256
R23	1	RESISTOR PAK 1K OHM SIP 6-PIN	829Ø21Ø
R24	1	RESISTOR 4.7K OHM 1/4 WATT 5%	82Ø7247
R25	1	RESISTOR 56Ø OHM 1/4 WATT 5%	82Ø7156
R26	1	RESISTOR 1ØK OHM 1/4 WATT 5%	82Ø731Ø
R27	1	RESISTOR PAK 4.7K OHM SIP 6-PIN	8293247
R28-35	8	RESISTOR 5Ø OHM 1/4 WATT 5%	82Ø7Ø51
R36	1	RESISTOR 1Ø OHM 1/4 WATT 5%	82Ø7Ø1Ø
R37	1	RESISTOR 4.7K OHM 1/4 WATT 5%	82Ø7247
R38	1	RESISTOR 56Ø OHM 1/4 WATT 5%	82Ø7156
R39	1	RESISTOR 22Ø OHM 1/4 WATT 5%	82Ø7122
R4Ø	1	RESISTOR PAK 22Ø/33Ø OHM SIP 8-PIN	829ØØ19
R41	1	RESISTOR 16K OHM 1/4 WATT 5%	82Ø7316
R42	1	RESISTOR 1ØK OHM 1/4 WATT 5%	82Ø731Ø
R43-45	3	RESISTOR PAK 22Ø/33Ø OHM SIP 1Ø-PIN	829ØØ2Ø

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(889613Ø)
REV. Ø9/Ø7/82 PAGE 3 OF 4

SYMBOL	QTY	DESCRIPTION	PART NO.
U1	1	IC 26SØ2 ONE SHOT	8Ø6ØØØ2
U2	1	IC 74LS193 DUAL CLOCK COUNTER	9Ø2Ø193
U3	1	IC 74S74 DUAL FLIP-FLOP	9Ø1ØØ74
U4	1	IC 74S51 AND OR INVERTER	9Ø1Ø051
U5-7	3	SOCKET 2Ø-PIN (DIP)	85Ø9ØØ9
U8	1	IC 74LS244 LINE DRIVERS	9Ø2Ø244
U9	1	SOCKET 2Ø-PIN (DIP)	85Ø9ØØ9
U1Ø	1	IC 74S74 DUAL FLIP-FLOP	9Ø1ØØ74
U11	1	SOCKET 2Ø-PIN (DIP)	85Ø9ØØ9
U12-14	3	IC 74S74 DUAL FLIP-FLOP	9Ø1ØØ74
U15	1	IC 74S86 QUAD 2-IN OR	9Ø1Ø086
U16	1	IC 74LS175 QUAD FLIP-FLOP	9Ø2Ø175
U17	1	SOCKET 18-PIN (DIP)	85Ø9ØØ6
U18	1	SOCKET 18-PIN (DIP)	85Ø9ØØ6
U19	1	IC 74LS14 HEX INVERTER	9Ø2ØØ14
U2Ø,21	2	IC 74S74 DUAL FLIP-FLOP	9Ø1ØØ74
U22	1	IC 74LS74 DUAL FLIP-FLOP	9Ø2ØØ74
U23	1	IC MPQ67ØØ TRANSISTOR PAK	818Ø7ØØ
U24	1	IC 74LS32 QUAD 2-IN OR	9Ø2ØØ32
U25	1	IC 74LS123 DUAL MULTIVIBRATOR	9Ø2Ø123
U26-28	3	IC 74LS191 COUNTER	9Ø2Ø191
U29	1	IC 74LS174 HEX FLIP-FLOP	9Ø2Ø174
U3Ø	1	IC 74SØØ QUAD 2-IN NAND	9Ø1ØØØØ
U31	1	IC DDU4-5Ø6Ø 6ØNS DELAY LINE	8429Ø16
U32	1	IC 74S124 DUAL OSCILLATOR	9Ø1Ø124
U33	1	IC 74SØ2 QUAD 2-IN NOR	9Ø1ØØØ2
U34	1	SOCKET 24-PIN (DIP)	85Ø9ØØ1
U35,36	2	IC MC3487 DRIVER	8Ø5Ø487
U37	1	IC 74LS54 AND OR INVERT	9Ø2ØØ54
U38	1	IC 74LSØ8 QUAD 2-IN AND	9Ø2ØØØ8
U39	1	IC 74S174 HEX FLIP-FLOP	9Ø1Ø174
U4Ø	1	SOCKET 24-PIN (DIP)	85Ø9ØØ1
U41	1	SOCKET 24-PIN (DIP)	85Ø9ØØ1
U42	1	SOCKET 5Ø-PIN (ZRF)	85Ø9Ø12
U43	1	IC 74LS74 DUAL FLIP-FLOP	9Ø2ØØ74
U44,45	2	IC 74S138 LINE DECODER	9Ø1Ø138
U46	1	IC 74SØ4 HEX INVERTER	9Ø1ØØØ4
U47	1	IC 74LS273 OCTAL FLIP-FLOP	9Ø2Ø273
U48,49	2	IC 74LS244 LINE DRIVERS	9Ø2Ø244

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(889613Ø)
REV. Ø9/Ø7/82 PAGE 4 OF 4

SYMBOL	QTY	DESCRIPTION	PART NO.
U5Ø	1	IC 74LS24Ø OCTAL BUFFER	9Ø2Ø24Ø
U51	1	IC 74LS54 AND OR INVERT	9Ø2ØØ54
U52	1	IC 74LS174 HEX FLIP-FLOP	9Ø2Ø174
U53	1	IC 74S64 AND OR INVERTER	9Ø1ØØ64
U54	1	IC MC3486 RECIEVER	8Ø5Ø486
U55	1	IC 74LS125 QUAD BUFFER	9Ø2Ø125
U56	1	IC 74S64 AND OR INVERTER	9Ø1ØØ64
U57	1	IC 74LSØ8 QUAD 2-IN AND	9Ø2ØØØ8
U58	1	IC 74SØ4 HEX INVERTER	9Ø1ØØØ4
U59	1	IC 74SØ8 QUAD 2-IN AND	9Ø1ØØØ8
U6Ø	1	IC 8T31 TRANSCIEVER	9Ø6ØØ31
U61	1	IC 74LS374 OCTAL FLIP-FLOP	9Ø2Ø374
U62	1	IC 74LS273 OCTAL FLIP-FLOP	9Ø2Ø273
U63,64	2	IC 7416 HEX INVERTER	9Ø1ØØ16
U65	1	IC 74S32 QUAD 2-IN OR	9Ø1ØØ32
U66,67	2	IC 74LS139 DUAL LINE DECODER	9Ø2Ø139
U68	1	IC 74S139 DUAL DECODER	9Ø1Ø139
U69	1	IC 74S138 LINE DECODER	9Ø1Ø138
U7Ø	1	IC 83Ø4 BUS TRANCIEVER	8Ø6Ø3Ø4
U71	1	IC 74LS244 LINE DRIVERS	9Ø2Ø244
U72	1	IC 7416 HEX INVERTER	9Ø1ØØ16
U73	1	IC 74LS244 LINE DRIVERS	9Ø2Ø244
U74	1	IC 74LS374 OCTAL FLIP-FLOP	9Ø2Ø374
U75	1	IC 74SØ4 HEX INVERTER	9Ø1ØØØ4
U76	1	IC 74LS221 DUAL MULTIVIBRATOR	9Ø2Ø221
U77	1	IC 78MØ5 +5V REGULATOR	8Ø518Ø5
U77	1	SCREW, #4-4Ø X 3/8" PPH	8569ØØ2
U77	1	NUT #4, KEPS	8579ØØ3
U77	1	HEAT SINK 6Ø7ØB	8549Ø11
U78	1	IC 75453 LAMP DRIVER	8Ø5Ø453
Y1	1	CRYSTAL 2Ø.Ø MHZ	84Ø9Ø24
Y2	1	CRYSTAL 8.ØØØ MHZ	84Ø9ØØ6

BILL OF MATERIAL
5 1/4" HARD DISK INTERFACE PC BOARD ASSY.(8898417)
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SYMBOL	QTY	DESCRIPTION	PART NO.
	1	PC BOARD (INTERFACE) " - "	85Ø9295
TP1-7	7	STAKING PINS	8529Ø14
ABC	3	STAKING PINS	8529Ø14
BCDE,FG	6	STAKING PINS	8529Ø14
HJK,STU	6	STAKING PINS	8529Ø14
VWX	3	STAKING PINS	8529Ø14
AC-AF	4	STAKING PINS	8529Ø14
AG-AK	4	STAKING PINS	8529Ø14
AL-AP	4	STAKING PINS	8529Ø14
C1-24	24	CAPACITOR .1 UF 5ØV MONO AXIAL	8374lØ4
C25	1	CAPACITOR lØ UF 16V ELEC. RAD.	8326lØ1
C26	1	CAPACITOR lØ UF 16V ELEC. AXIAL	8316lØ1
C27-55	29	CAPACITOR .1 UF 5ØV MONO AXIAL	8374lØ4
C56	1	CAPACITOR 47 UF 16V ELEC. AXIAL	8316471
C57	1	CAPACITOR 47 UF 16V ELEC. AXIAL	8316471
C58	1	CAPACITOR 33 UF 5ØV ELEC. AXIAL	8316334
C59-62	4	CAPACITOR .1 UF 5ØV MONO AXIAL	8374lØ4
J2	1	CONNECTOR 5Ø-PIN RGHT.ANG. LATCH	8519147
R1-3	3	RESISTOR 51 OHM 1/4WATT 5%	82Ø7Ø51
R4	1	RESISTOR 4.7K OHM 1/4WATT 5%	Ø2Ø7247
R5	1	RESISTOR 1K OHM 1/4WATT 5%	82Ø721Ø
R6	1	RESISTOR 4.7K OHM 1/4WATT 5%	82Ø7247
R7	1	RESISTOR 4.7K OHM 1/4WATT 5%	82Ø7247
R8	1	RESISTOR 1ØØ OHM 1/4WATT 5%	82Ø711Ø
R9-13	5	RESISTOR 4.7K OHM 1/4WATT 5%	82Ø7247
RP1	1	RESISTOR PAK 39 OHM DIP	829ØØØ2
U1-8	8	SOCKET 16-PIN	85Ø9ØØ3
U13	1	SOCKET 2Ø-PIN	85Ø9ØØ9
U2Ø	1	SOCKET 16-PIN	85Ø9ØØ3
U22	1	SOCKET 28-PIN	85Ø9ØØ7
U26	1	SOCKET 16-PIN	85Ø9ØØ3
U4Ø	1	SOCKET 2Ø-PIN	85Ø9ØØ9

BILL OF MATERIAL
5 1/4" HARD DISK INTERFACE PC BOARD ASSY.(8898417)
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SYMBOL	QTY	DESCRIPTION	PART NO.
U1-8	8	IC MK4116 RAM	8Ø41Ø16
U9	1	IC 74SØ4 HEX INVERTER	9Ø1ØØ4
U1Ø	1	IC 74LSØØ QUAD 2-IN NAND	9Ø2ØØØ
U11	1	IC DDU-2ØØ DELAY 2ØØ NS	8429ØØ4
U12	1	IC 74LS24Ø OCTAL BUFFER	9Ø2Ø24Ø
U13	1	IC 83Ø4 8 BIT BUS DRIVER	8Ø6Ø3Ø4
U14	1	IC 74LS244 OCTAL BUFFER	9Ø2Ø244
U15	1	IC 74LS244 OCTAL BUFFER	9Ø2Ø244
U16	1	IC 74S74 DUAL FLIP-FLOP	9Ø1Ø074
U17	1	IC 74S11 TRIPLE 3-IN AND	9Ø1Ø011
U18	1	IC 74SØ4 HEX INVERTER	9Ø1ØØ04
U19	1	IC 74SØØ QUAD 2-IN NAND	9Ø1ØØØØ
U2Ø	1	IC 8T26 4 BIT BUS DRIVER	9Ø6ØØ26
U21	1	IC 74157 QUAD	9ØØØ157
U22	1	IC Z8Ø CTC	8Ø47882
U23	1	IC 74S32 QUAD 2-IN OR	9Ø1Ø032
U25	1	IC 74SØ2 QUAD 2-IN NOR	9Ø1ØØ02
U26	1	IC 8T26 4 BIT BUS DRIVER	9Ø6ØØ26
U27	1	IC 74157 QUAD	9ØØØ157
U28	1	IC 74S138 DECODER	9Ø1Ø138
U29	1	IC 74SØ4 HEX INVERTER	9Ø1ØØ04
U3Ø	1	IC 74S139 DECODER	9Ø1Ø139
U31	1	IC 74SØ4 HEX INVERTER	9Ø1ØØ04
U32	1	IC 74LS14 HEX INVERTER	9Ø2ØØ14
U33	1	IC 74LS174 HEX FLIP-FLOP	9Ø2Ø174
U34	1	IC 74LS138 DECODER	9Ø2Ø138
U35	1	IC 74LS273 FLIP-FLOP	9Ø2Ø273
U36	1	IC 74SØ8 QUAD 2-IN AND	9Ø1ØØ08
U37	1	IC 74LS133 13-IN NAND	9Ø2Ø133
U38	1	IC 74S64 AND-OR-INVERT	9Ø1Ø064
U39	1	IC 7438 QUAD 2-IN NAND	9ØØØ038
U4Ø	1	IC 83Ø3 8 BIT BUS DRIVER	8Ø6Ø3Ø3
U41-43	3	IC 74LS24Ø OCTAL BUFFER	9Ø2Ø24Ø
VR1	1	REGULATOR 79LØ5 -5V	8Ø519Ø5

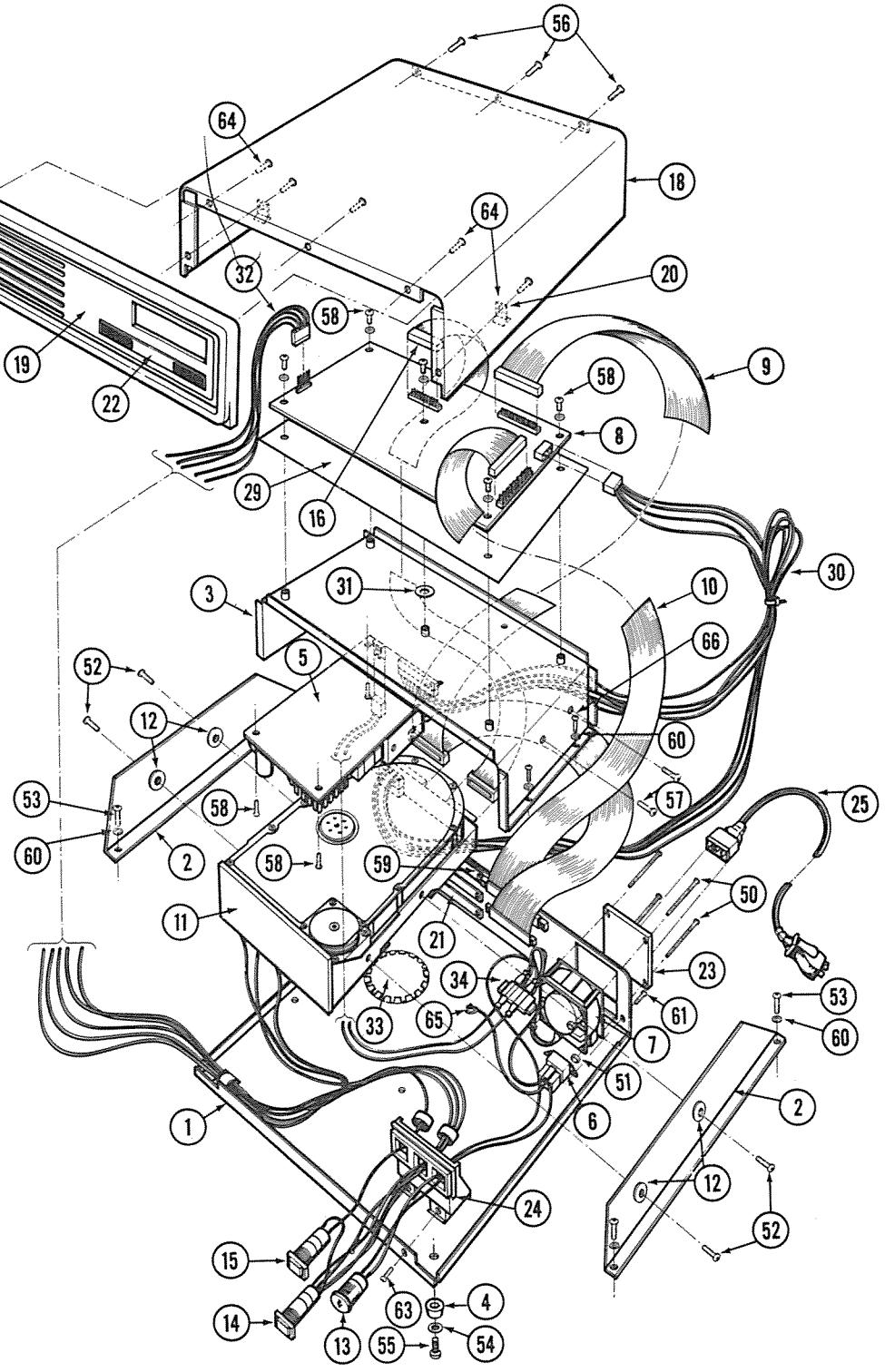
PARTS LIST - 15 Meg Hard Disk Drive Assembly 26-4155

Item	Sym	Description	Part Number
1	1	Case, Bottom	878927Ø
2	2	Mount, Disk Drive	8729179
3	1	Chassis Bracket, PS Mounting	872918Ø
4	4	Foot	859Ø123
5	1	Power Supply Assy. 65 W	879ØØ49
6	1	Harness Assembly, AC	87Ø9332
7	1	Fan Assembly	879Ø4Ø1
8	1	PCB Assembly, Controller	8896ØØ
9	1	Cable Assy., Internal Control	87Ø933Ø
1Ø	1	Cable Assy., To External Drives	87Ø94Ø1
11	1	Drive Assembly, 15 Meg HD	879Ø2Ø5
12	4	Grommet, Rubber	859Ø127
13	1	Switch, Keylock	8489Ø47
14	1	Switch, Pushbutton ON/OFF	8489Ø48
15	1	Indicator Light	8469ØØ9
16	1	Cable Assy., Internal Data	87Ø9324
17	1	Cable Assy, Ext. Control (not shown)	87Ø9329
18	1	Cover, Top	8729269
19	1	Bezel, Front	8719Ø39
2Ø	2	Clip, Grounding	8559Ø4Ø
21	3	Plate, Cover	8729274
22	1	Logo, Strip	8719358
23	1	Fan Guard/Filter	8719298
24	1	Bezel, Switch	871923Ø
25	1	Power Cord, AC	87Ø9Ø57
26	1	PCB Assy., Interface (not shown)	8898417
27	1	Cable Assy., Internal Computer (not shown, not applicable to Models 12, 16B)	_____
28	1	Plate, Connector Mounting (not shown, not applicable to Models 12, 16B)	_____
29	1	Insulator, Mylar	_____
3Ø	1	Harness Assembly, DC	87Ø9334
31	1	Washer, Plastic	8589Ø72
32	1	Harness Assy., Write Protect	87Ø9347
33	1	Cover Plate, Access	8729272
34	1	Terminal Strip (on AC harness)	_____
35-49		Not Used	

PART LIST - 15 Meg Hard Disk Drive Assembly 26-4155

Item	Sym	Description	Part Number
5Ø	4	Screw, #6-32 x 2-1/4" F.H.	8569161
51	4	Nut, #6-32 Hex	8579ØØ4
52	4	Screw, #6-32 x 3/16" Shoulder	8569171
53	4	Screw, #6-32 x 1/4" PPH	856916Ø
54	4	Washer, #1Ø Flat	8589Ø74
55	4	Screw, #1Ø x 1/2" Sheet Metal	8569Ø62
56	3	Screw, #6 x 3/8" Blk. Ox. PPH	8569Ø26
57	2	Screw, #1Ø x 1/4" Sheet Metal	8569153
58	7	Screw, #6 x 1/4" SEMS PPH	856916Ø
59	8	Screw, #4 x 1/4" PPH Sht. Met.	856912Ø
6Ø	11	Lockwasher, #6 Internal Lock (3 not shown, mount on item 56)	
61	2	Screw, #4-4Ø x 1/2" PPH	8569Ø33
62	2	Nut, #4-4Ø Hex Locking (not shown, mounts on 61)	8579ØØ3
63	2	Screw, #6 x 5/16" PPH Plast.	8569lØ7
64	5	Screw, #8-34 x 3/8" Plastite	8569lØ7
65	1	Nut, 36-32 w/Lockwasher	8579ØØ4
66	4	Screw, #6-32 x 1/4" PPH	856916Ø
67	4	Screw, #4-4Ø x 3/4" PPH Zinc (not shown, mounts into back plate of item 1)	8569Ø59
68	4	Washer, #4 Star Ext Tooth (not shown, mounts on item 67)	8589Ø75
69	4	Nut, #4-4Ø Lock (not shown, mounts on item 68)	8579ØØ3
7Ø	5	Washer, #8 Ext. Star (not shown, mounts under item 18)	

Exploded View, 12/15 Meg Hard Disk Assembly



PARTS LIST

Power Supply Assembly 879ØØ49, 65W

Item	Sym	Description	Part Number
1	1	Printed Circuit Board	87Ø9365
1	J1	Fan Output 2-pin verticle	8519214
	BR1	Bridge, 2A, 6ØØPIV	816Ø4Ø2
	C1	1ØµF, 35V, elect., radial	8326ıØ3
	C2	4.7µF, 5ØV, elect., radial	8325474
	C3	Ø.Ø47µF, 5Ø/63V stacked metal	8393474
	C4	Ø.47µF, 5Ø/63V stacked metal	8394474
	C5	Ø.Ø68µF, 5Ø/63V stacked metal	8393684
	C6	1µF, 5Ø, elect., radial	8325Ø14
	C7	Ø.ØØ1µF, 63V poly	8392ıØ4
	C8	47µF, 25V, elect., radial	8326472
	C9	1µF, 5ØV, elect., radial	8325Ø14
	C1Ø	22ØØµF, 1ØV, elect., radial	8328224
	C11	22ØØµF, 1ØV, elect., radial	8328224
	C12	22ØØµF, 6.3V, elect., radial	832822Ø
	C13	Ø.Ø1µF, 5Ø/63V stacked metal	8393ıØ4
	C14	1ØØµF, 35V, elect., radial	8327ıØ3
	C15	1ØØØpF, 1ØØV, ceramic disc	83Ø2ıØ6
	C16	22ØØµF, 16V, elect., radial	8328221
	C17	Ø.1µF, 5Ø/63V stacked metal	83Ø4ıØ4
	C18	33ØØµF, 16V, elect., radial	8328331
	C19	1ØØµF, 35V, elect., radial	8327ıØ3
	C2Ø	1ØØµF, 25V, elect., radial	8327ıØ2
	C21	.Ø47µF, 5Ø/63V stacked metal	8393474
	C22	.Ø1µF, 5Ø/63V stacked metal	8393ıØ4
	C23	47ØµF, 16V, elect., radial	8327461
	C24	Ø.1µF, 25ØVDC metal poly	8394ıØ6
	C25	22ØØµF, 16V, elect., radial	8328221
	C26	22ØµF, 2ØØV, elect., radial	8327226
	C27	Not Used	
	C28	47ØØ pF, 125VAC, ceramic disc	83Ø3475
	C29	22ØµF, 2ØØV, elect., radial	8327226
	C3Ø	47ØØpF, 125VAC, ceramic disc	83Ø3475
	C31	47ØØpF, 125VAC, ceramic disc	83Ø3475
	C32	.22µF, 125VAC, ceramic disc	8393432
	C33	.Ø1µF, 25ØVAC, metal paper	8393ıØ6
	C34	Not Used	
	C35	Not Used	
	C36	.ØØ1µF, 5Ø/63V stacked metal	8392Ø14
	C37	.ØØ1µF, 63ØV, poly	8392Ø17
	C38	.Ø22µF, 63V, poly	8393422

PARTS LIST

Power Supply Assembly 879ØØ49, 65W

Item	Sym	Description	Part Number
	C39	.Ø22µF, 63V, poly	8393422
	CR1	Diode, 1N4148, switching	815Ø148
	CR2	Diode, 1N4ØØ2, 1A/5ØPIV	815ØØØ2
	CR3	Diode, 1N4ØØ2, 1A/5ØPIV	815ØØØ2
	CR4	Diode, 1N4934, 1A/1ØØPIV	815Ø934
	CR5	Diode, MBR1Ø35, 8/1ØA, 35V, TO-22Ø	815ØØ35
	CR6	Diode, MUR81Ø, 8A/1ØØPIV, TO-22Ø	815Ø81Ø
	CR7	Diode, 1N4934, 8A/1ØØPIV	815Ø934
	CR8	MUR81Ø, 8A/1ØØPIV, TO-22Ø	815Ø81Ø
	CR9	Not Used	
	CR1Ø	Diode, 1N4ØØ2, 1A/5Ø PIV	815ØØØ2
	CR11	Diode, 1N4ØØ2, 1A/5Ø PIV	815ØØØ2
	F1	3 amp, AGC	8479104
	L1	Inductor, 5.Øµh, 1ØA	8419ØØ6
	L2	Inductor, 3Øµh, 5A	8419ØØ8
	L3	Not Used	
	L4	Inductor, 3Øµh, 5A	8419ØØ8
	L5	Inductor, 1ØØµh, 3A	8419ØØ9
	Q1	Transistor, MPSU51A, PNP, TO-2Ø2	81ØØØ51
	Q2	Transistor, MPSA55, PNP, TO-92	81ØØØ55
	Q3	Transistor, MPSUØ1A, NPN, TO-2Ø2	8111ØØ1
	Q4	Transistor, MPSU51A, PNP, TO-2Ø2	81ØØØ51
	Q5	Transistor, MPSUØ1A, NPN, TO-2Ø2	8111ØØ1
	Q6	SCR, 8A/5ØPIV, TO-22Ø	814Ø122
	Q7	Transistor, MJE13ØØ6, NPN, 8A, 4ØØV	811ØØØ6
	Q8	Transistor, MPSA55, PNP, TO-92	81ØØØ55
	Q9	Transistor, MPSAØ5, NPN, TO-92	811ØØØ5
	U1	IC, MC34Ø6Ø Switching Regulator or	8Ø6ØØ6Ø
		IC, µA/TL494 Switching Regulator	8Ø6Ø494
	U2	IC, Opto-isolator, 4N35	817ØØ35
	U3	IC, µA/TL431, Positive Shunt Reg.	8Ø6Ø428
	R1	Resistor, 1K, 1/4W, 5%	82Ø721Ø
	R2	Resistor, 68 ohm, 1/4W, 5%	82Ø7Ø68
	R3	Resistor, 28K, 1/4W, 1%	82ØØ328
	R4	Resistor, 39K, 1/4W, 5%	82Ø7339
	R5	Resistor, 15K, 1/4W, 5%	82Ø7315

PARTS LIST

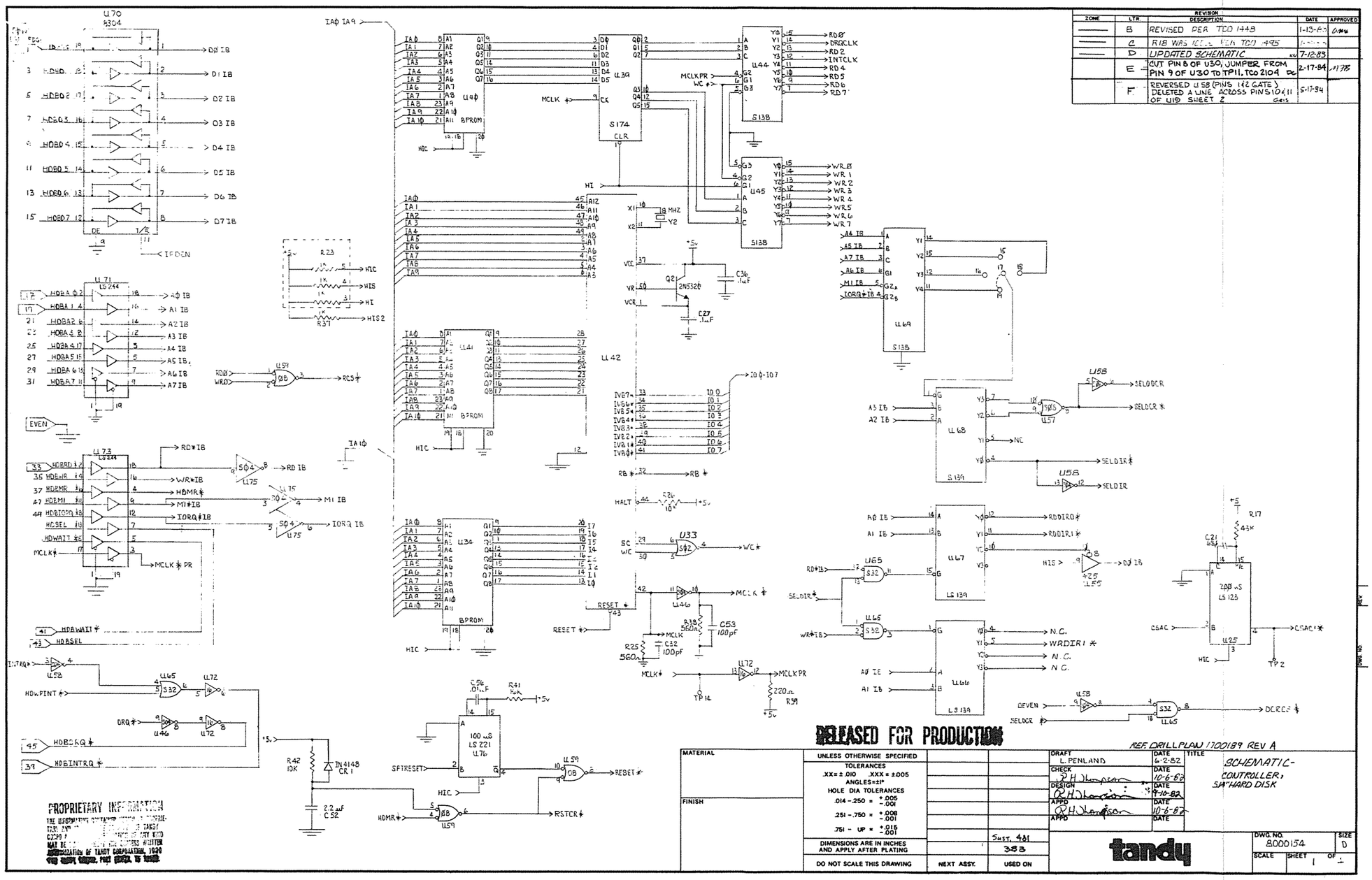
Power Supply Assembly 879ØØ49, 65W

Item	Sym	Description	Part Number
	R6	Resistor, 4.7K, 1/4W, 5%	82Ø7247
	R7	Resistor, 1ØK, 1/4W, 5%	82Ø731Ø
	R8	Resistor, 22K, 1/4W, 5%	82Ø7322
	R9	Resistor, 4.7K, 1/4W, 5%	82Ø7247
	R1Ø	Resistor, 4.7K, 1/4W, 5%	82Ø7247
	R11	Resistor, 1ØØ ohm, 1/4W, 5%	82Ø711Ø
	R12	Not Used	
	R13	Resistor, 18K, 1/4W, 5%	82Ø7318
	R14	Resistor, 33Ø ohm, 1/4W, 5%	82Ø7133
	R15	1K, 2Ø%, linear Pot.	8279211
	R16	Resistor, 3.32K, 1/4W, 1%	82ØØ232
	R17	Resistor, 1ØØ ohm, 1/4W, 5%	82Ø711Ø
	R18	Resistor, 1Ø ohm, 1/4W, 5%	82Ø71Ø
	R19	Resistor, 1 ohm, 1/4W, 5%	82Ø7ØØ1
	R2Ø	Resistor, 1ØK, 1/4W, 5%	82Ø731Ø
	R21	Resistor, 15Ø ohm, 1/4W, 5%	82Ø7115
	R22	Resistor, 33Ø ohm, 1/4W, 5%	82Ø7133
	R23	Resistor, 27 ohm, 2W, 1Ø%	8248127
	R24	Resistor, 22 ohm, 1/2W, 5%	8217Ø22
	R25	Resistor, 22K, 1/4W, 5%	82Ø7322
	R26	Resistor, 56K, 1W, 5%	8247356
	R27	Resistor, 39ØK, 1/4W, 5%	82Ø7439
	R28	Resistor, 22 ohm, 1/4W, 5%	82Ø7Ø22
	R29	Resistor, 28K, 1/4W, 1%	82ØØ328
	R3Ø	Resistor, 6.65K, 1/4W, 1%	82ØØ266
	R31	Not Used	
	R32	Resistor, 1K, 1/4W, 5%	82Ø721Ø
	R33	Resistor, 1ØØ ohm, 1/4W, 5%	82Ø711Ø
	R34	Resistor, 1K, 1/4W, 5%	82Ø721Ø
	R35	Resistor, 68 ohm, 1/4W, 5%	82Ø7Ø68
	R36	Resistor, 1ØØ, 1/4W, 5%	82Ø711Ø
	R37	Resistor, Ø.22 ohm, 2W, 1Ø%	8248Ø22
	R38	Thermistor 1Ø ohm 25c	8298Ø1Ø
	R39	Resistor, 56K, 1W, 5%	8248356
	R4Ø	Resistor, 82 ohm, 5W, 5%	8248Ø82
	R41	Resistor, 56K, 1/4W, 5%	82Ø7356
	R42	Resistor, 4.7K, 1/4W, 5%	82Ø7247
	T1	Transformer, Power, 65W flyback	879ØØ63
	T2	Line Choke, 5.5mH/side, 2A	879ØØ45
	VR2	Zener, 1N5232B, 5.6V	815Ø232
	VR1	Zener, 1N5256B, 3ØV	815Ø256
	VR3	Voltage Regulator 79M12 -12V	8Ø51912

MISCELLANEOUS HARDWARE

2	Clip, Fuse, PC Mount 1/4" Fuse (F1)	8559Ø42
1	Connector, 2 Pin, Vert. (J1)	8519214
1	Connector, 3 Pin (J3)	8519153
1	Connector, 13 Pin (J2)	8519154
1	Bracket, Heatsink, TO-22Ø (CR5,6,8)	8729167
1	Heatsink, Transistor, TO-22Ø (Q7)	8549ØØ3
4	Insulator, TO-22Ø, Mica (Q7,CR5,6,8)	8539ØØ3
4	Nut, KEPS, #4-4Ø (Q7,CR5,6,8)	8579ØØ3
4	Screw, #4-4Ø x 3/8" (Q7, CR5,6,8)	8569ØØ2
4	Washer, Shoulder (Q7, CR5,6,8)	8589Ø26
4	Wire, Jumper 2Ø Ga. (W1,2,5,6) .5"	
1	Wire, Jumper 2Ø Ga. (W7)	
1	Wire, Jumper 2Ø Ga. (W4)	
1	Wire, Stranded 6ØØV (W3)	8433ØØ6

13/ Schematics



R43 — LINE TERMINATORS 220/330
9 HDBD Ø
8 HDBD 1
7 HDBD 2
6 HDBD 3
5 HDBD 4
4 HDBD 5
3 HDBD 6
2 HDBD 7

R44 — LINE TERMINATORS 220/330
2 HDBA Ø
3 HDBA 1
4 HDBA 2
5 HDBA 3
6 HDBA 4
7 HDBA 5
8 HDBA 6
9 HDBA 7

R45 — LINE TERMINATORS 220/330
2 HDBRD*
3 HDBWR*
4 HDBMR*
7 HDBM1*
8 HDBIORQ*

4 PIN J8
1 +12v
2 + C62 47uF
3 +5v
4 C54 100uF, + C17 100uF

LL61 LS 374
AØ IB, A1 IB, A2 IB, CSAC, CRCOK, WR* IB, EDONE, ROVF* → DØ–D7
RD2 → OE
MCLK → CK
Q0–Q7 → IO Ø – IO 7

WR*IB, DCRCS* → LS32 LL24 → BIC*
RD*IB → LS32 LL24 → BOC*

LL58 → WR6, RD6

LL60Ø 8T31
DØ IB – D7 IB → D0–D7
MCLK → MCLK
ME
BIC, BOL
WC, RC
Q0–Q7 → IOØ – IO 7
24 → +5v
12

RCS* → LL27 LS 191
IOØ, IO1, IO2, IO3 → D0–D3
HIS → D/U
MCLK → CK
QA–QD → RA Ø – RA 3

RCS* → LL28 LS 191
IO4, IO5, IO6, IO7 → D0–D3
WR2 → CK
QA–QD → RA 4 – RA 7

RCS* → LL26 LS 191
IOØ, IO1 → D0, D1
MCLK → CK
QA, QB → RA8, RA9
QC → ROVF*

IO2, IO3, IO4, IO5, IO6, IO7 → LL29 LS 174
WR7 → CK
HIC → CLR
Q0 → WAEN*
Q1 → CRCIZ*
Q2 → RGATE
Q3 → WRITE*
Q4 → IBLAT
Q5 → CRCH

RA Ø – RA 9 → LL17 Z114 → IO Ø – IO 3
WC* → WE

RA Ø – RA 9 → LL18 Z114 → IO 4 – IO 7
WC* → WE
RB* → CE

IO Ø – IO 7 → LL62 LS 273
WR1 → CP
RESET* → MR
LL63 → HSEL Ø, HSEL 1, HSEL 2
LL64 → DR54, DR53, DR52, DR51

SOWP* → LL59 → WGI
LL64 → WGI*, RWC*, STEP, DIR IN
IO Ø – IO 5 → LL52 LS 174
WR1 → CP
RESET* → MR

Z2Ø–33Ø R40 → +5v
IO Ø – IO 7 → LL74 LS 374
MCLK → CP
RDS → OE
TP12
IND FX, READY*, WF*, SC*, TRE Ø*
DRSEL*, DRUN*, HFRQ*

LL22 LS 74
S, D, CK → HIS
U19 LS14
WR3

J5 34PIN: 14, 18, 4, 26, 28, 3Ø, 32, 6, 24, 34, 20, 22, 12, 8, 1Ø — ALL ODD
J6 50PIN: 14, 18, 4, 26, 28, 3Ø, 32, 4Ø, 2, 36, 34, 20, 22, 12, 8, 1Ø — ALL ODD

IORQ IB, SELDCR → LL27 S02
DEVEN, RD IB → S64 LL56
SELDTR → LL56
MI IB → LL56
LL56 → HDSEL
LL58 → IFDEN
TP 13

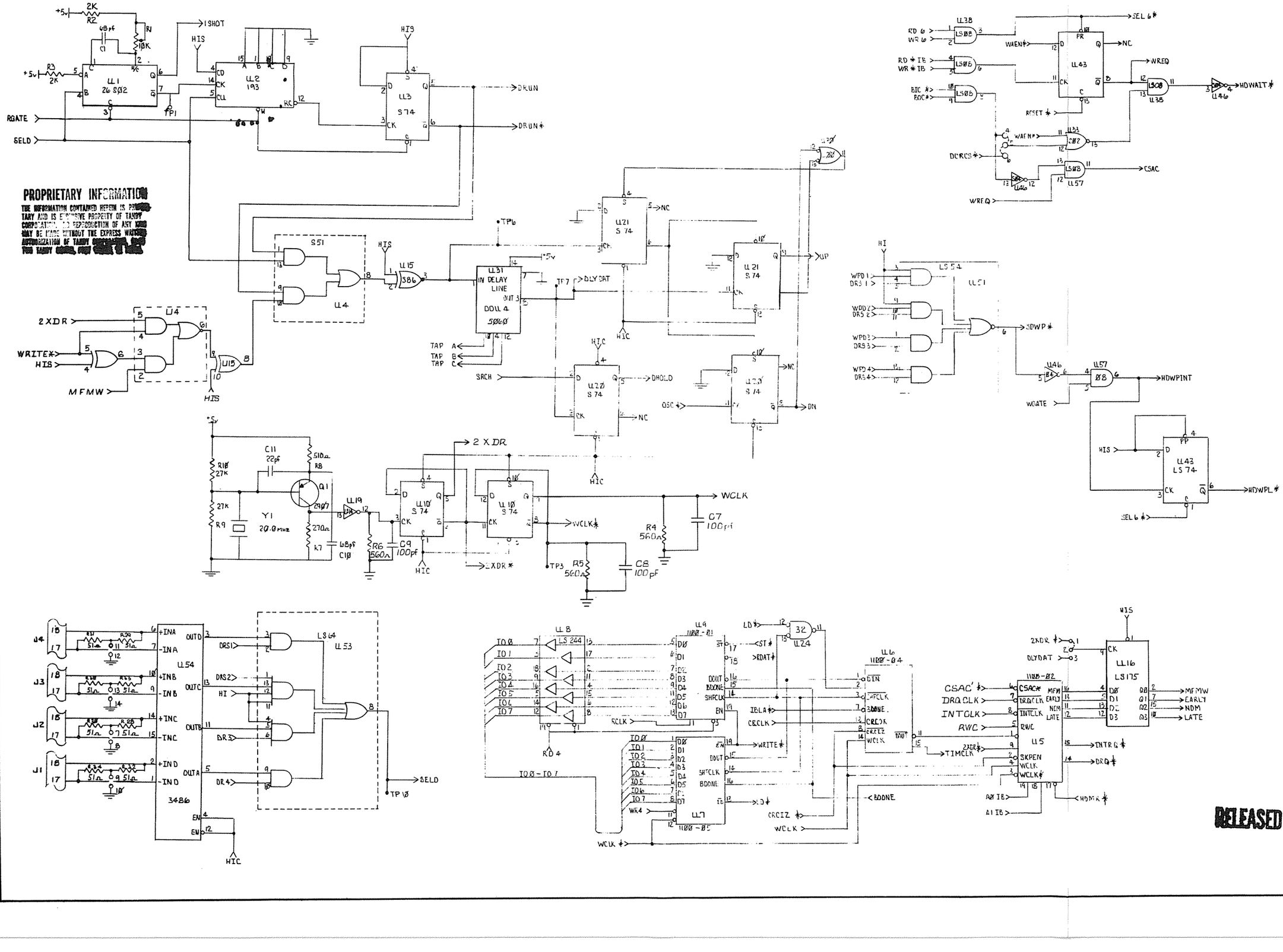
R36 15Ω +12v
J1 J2 J3 J4 (7 7 7)
DRSEL* → 1 2 4 6 8 11 12 15 16 19 20

R27 4.7K
WPD1, WPD2, WPD3, WPD4
WPD1* (Ø1-PE), WPD2* (Ø2-PE), WPD3* (Ø3-PE), WPD4* (Ø4-PE)
NC, NC, HDWPL*, INTRQ*
LL50 LS240
LL49 LS 244
D7 IB – D0 IB
RDDIR*

DEVEN
WAITEN IB
SFTRESET
RSTCR*
DØ IB – D7 IB → LL47 LS 273 → LL48 LS 244 → DØ IB – D7 IB
WRDIR1*
RDDIR1*

DWG NO	REV
8000154	
SCALE	SHEET 2 OF 4

TELEDYNE KOP H1417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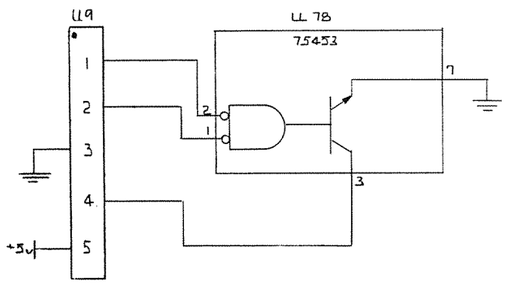
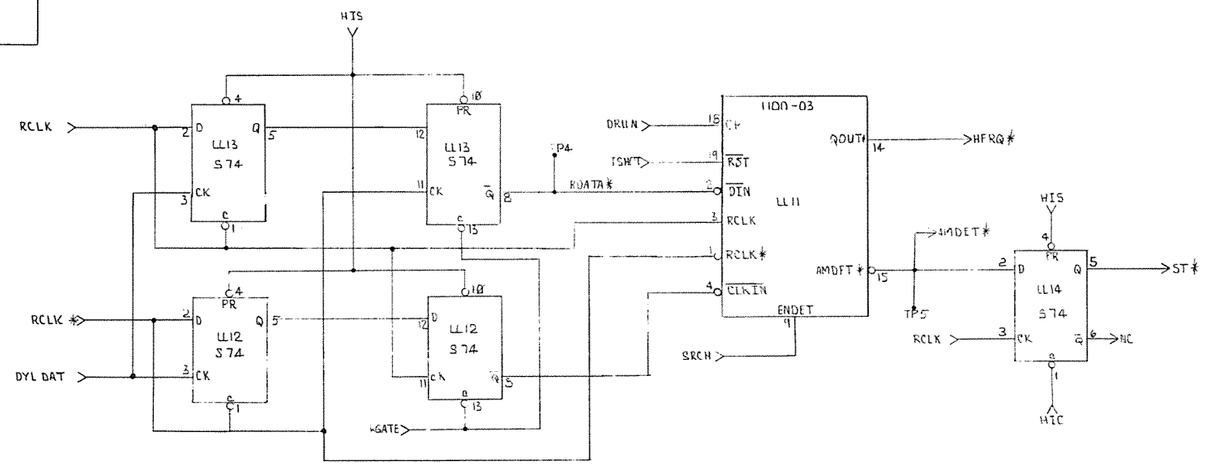
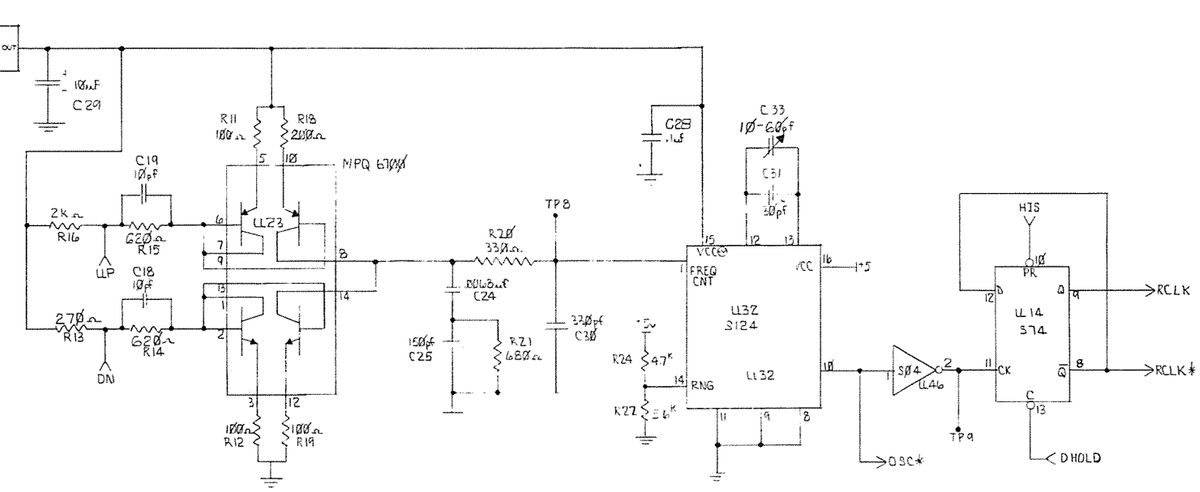
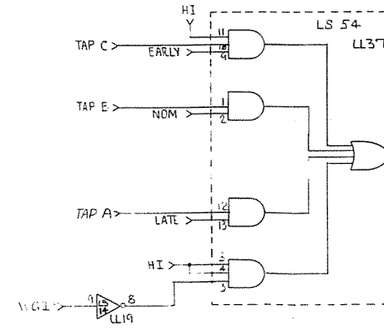
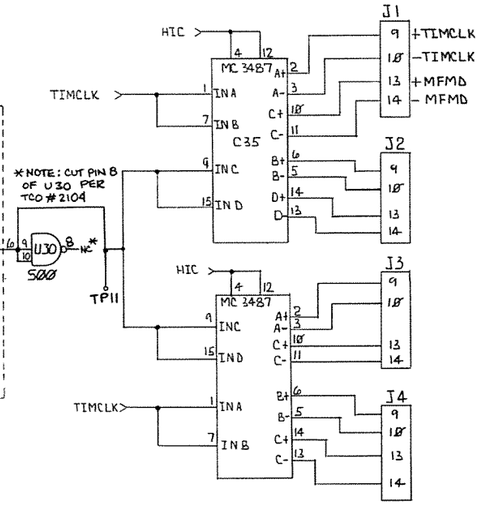
RELEASED FOR PRODUCTION
DWG NO 8000154
SCALE
SHEET 3 OF 4











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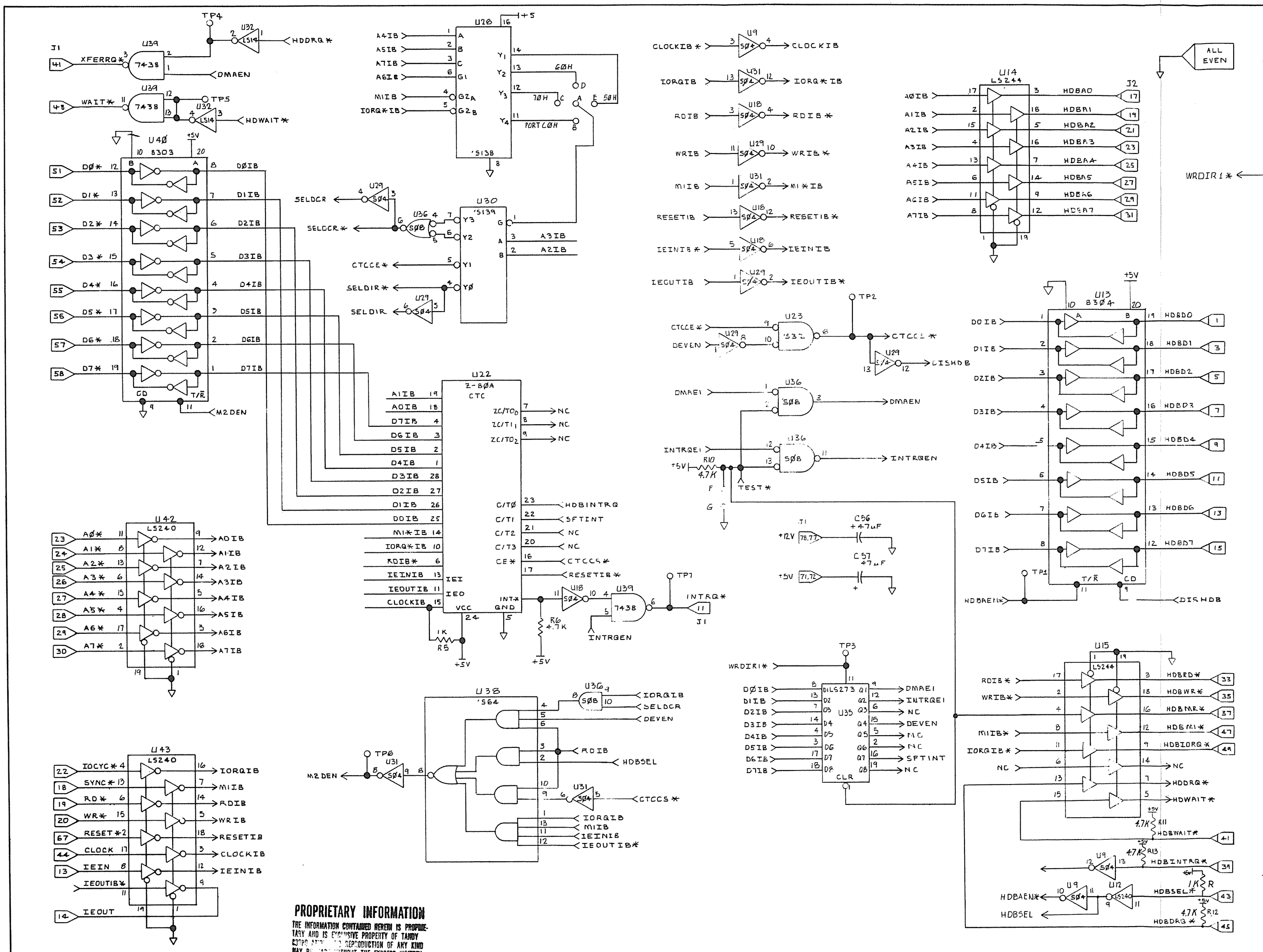
DWG NO	REV
8000154	
SCALE	SHEET 4 OF 4

LETTER	REVISION	DATE	APPROVED
—	RELEASED FOR PRODUCTION	12-22-82	WHH
—	SCHEMATIC UPDATED	7-12-83	
A	DELETED RESETIB* FROM U15-4, U35-1 AND ADDED A CIRCUIT FROM U15-4 (U35-1 TO R10 TCO# 2320	4-27-84	



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RELEASED FOR PRODUCTION

REF. DRILLPLAN 1700192

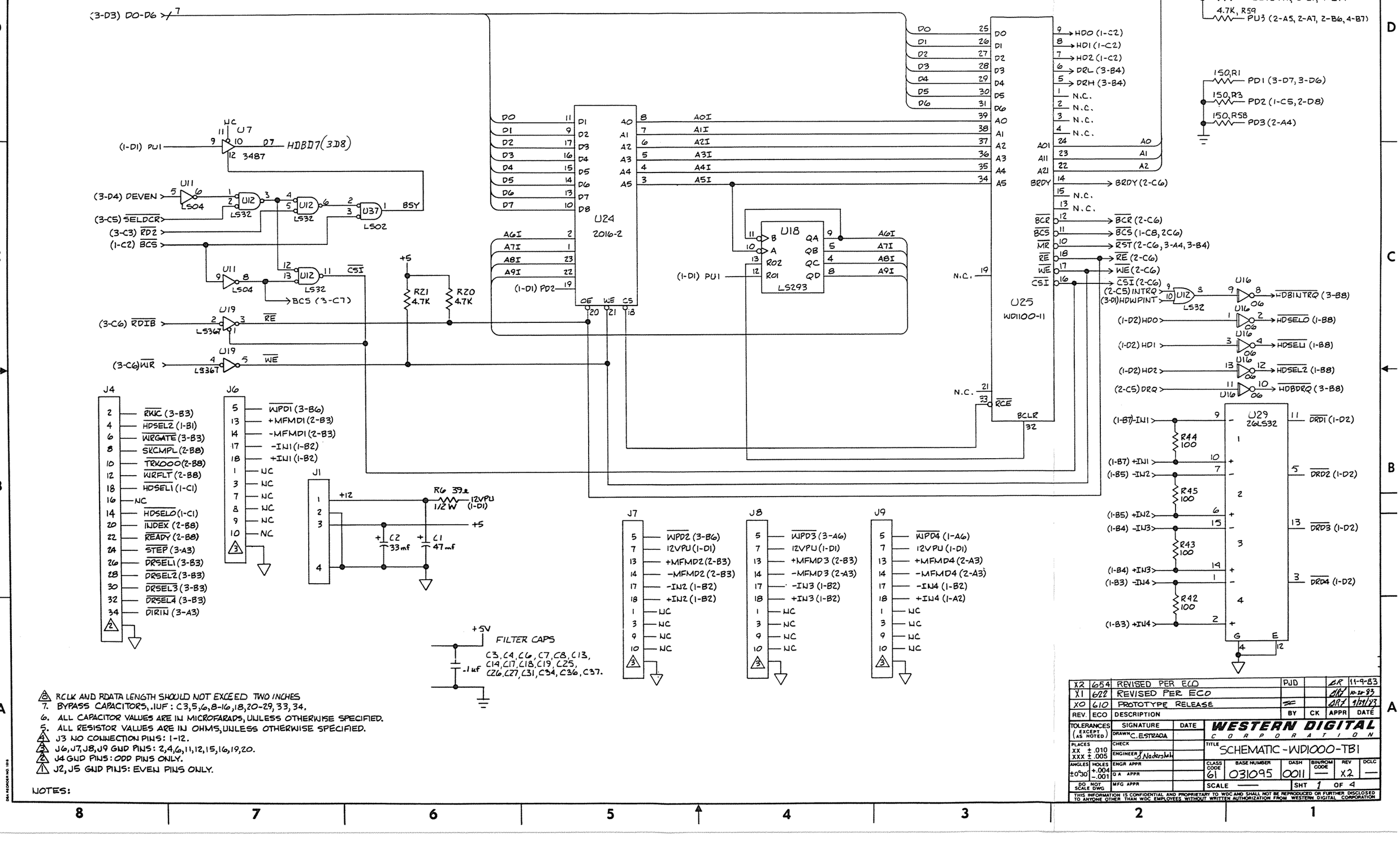
DRAFT	DATE	TITLE	SCHEMATIC - 5 1/4" HARD DISK INTERFACE
CHECK R.H. Thompson	DATE 12/22/82		
DESIGN R.H. Thompson	DATE 12/22/82		
APPD W. Atwell	DATE 12/22/82		
tandy	DWG NO 8000143	SIZE D	
	SCALE N/A	SHEET 1	OF 2

STANDARD CONFIGURATION AP-AK

200NS DELAY LINE 20ns / TOP Zo = R_L

RELEASED FOR PRODUCTION

DWG NO	SIZE
8000-143	D
SCALE: Ø	SHEET 2 OF 2



△5 RCLK AND RDATA LENGTH SHOULD NOT EXCEED TWO INCHES
7. BYPASS CAPACITORS, .1UF: C3,5,6,8-16,18,20-29,33,34.
6. ALL CAPACITOR VALUES ARE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
5. ALL RESISTOR VALUES ARE IN OHMS, UNLESS OTHERWISE SPECIFIED.
△4 J3 NO CONNECTION PINS: 1-12.
△3 J6, J7, J8, J9 GND PINS: 2,4,6,11,12,15,16,19,20.
△2 J4 GND PINS: ODD PINS ONLY.
△1 J2, J5 GND PINS: EVEN PINS ONLY.

NOTES:

REV.	ECO	DESCRIPTION	BY	CK	APPR	DATE
X2	654	REVISED PER ECO	PJD		DR	11-9-83
X1	622	REVISED PER ECO			DR	10-26-83
X0	610	PROTOTYPE RELEASE			DR	9/29/83

TOLERANCES (EXCEPT AS NOTED): PLACES XX ± .010, XXX ± .005; ANGLES ±0°30'; HOLES +.004 −.001; DO NOT SCALE DWG.

	SIGNATURE	DATE
DRAWN	C. ESTRADA	
CHECK		
ENGINEER		
ENGR APPR		
Q A APPR		
MFG APPR		

WESTERN DIGITAL CORPORATION

TITLE: SCHEMATIC - WD1000-TB1

CLASS CODE	BASE NUMBER	DASH	BIN/ROM CODE	REV	DCLC
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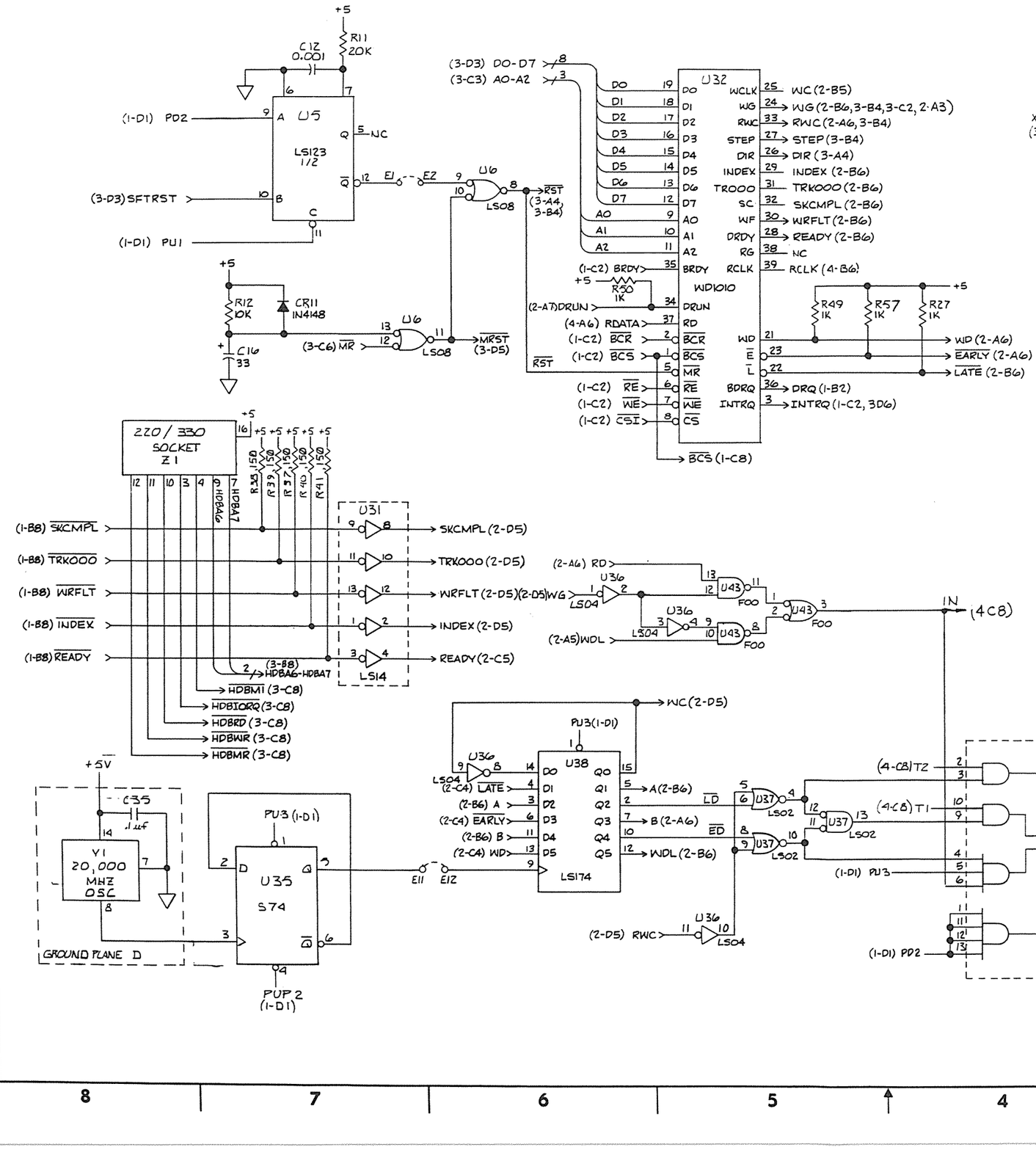
SCALE — SHT 1 OF 4

DRA RECORDER NO. 1818



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TOLERANCES (EXCEPT AS NOTED)	SIGNATURE	DATE
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PLACES XX ±.010 XXX ±.005	CHECK	
ANGLES ±0°30'	ENGINEER	
HOLES +.004 −.001	ENGR APPR	
DO NOT SCALE DWG	Q A APPR	
	MFG APPR	

WESTERN DIGITAL CORPORATION

TITLE: WD1000-TB1

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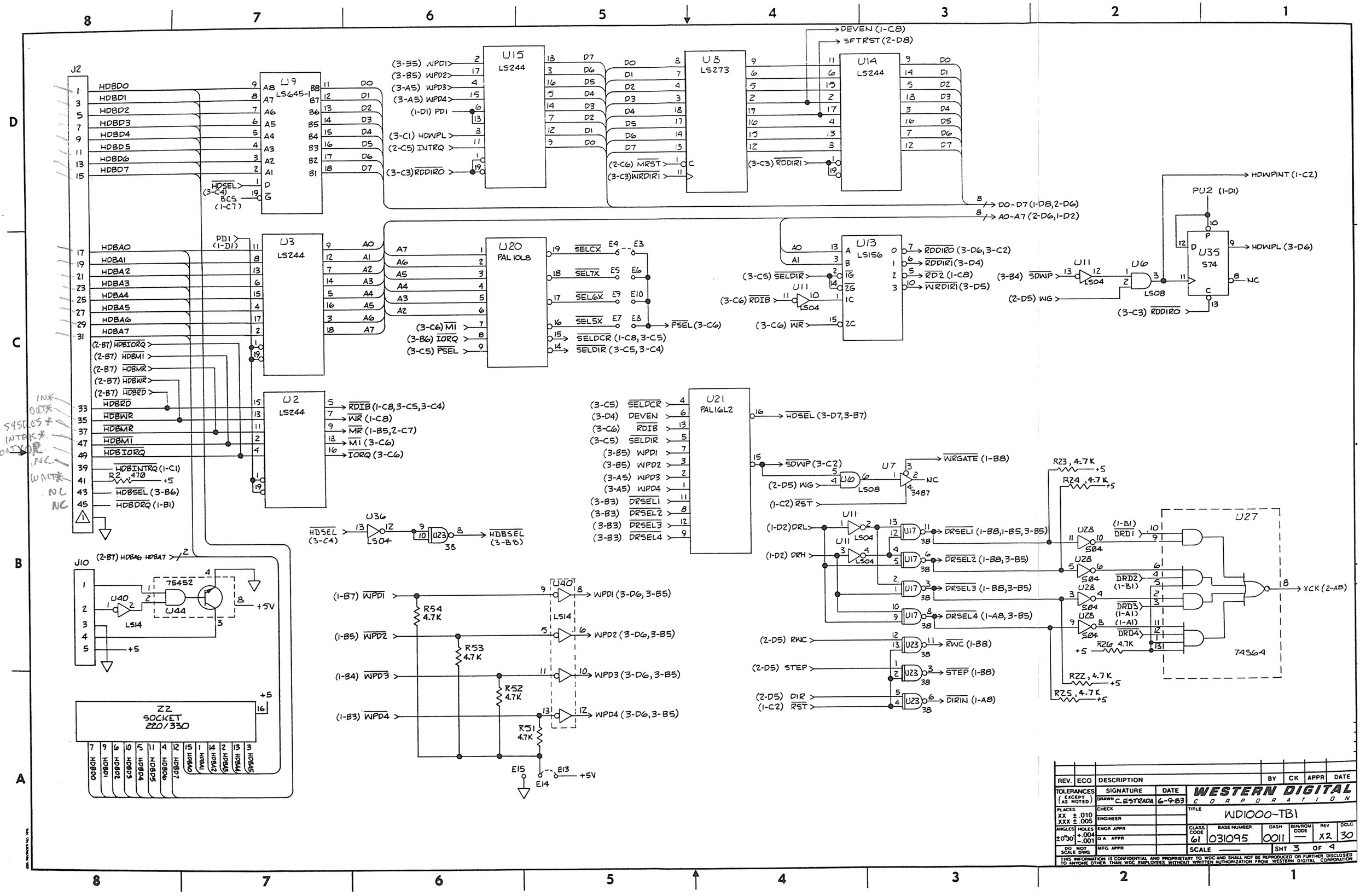
SCALE —— SHT 2 OF 4



REV.	ECO	DESCRIPTION	BY	CK	APPR	DATE

TOLERANCES (EXCEPT AS NOTED)	SIGNATURE	DATE
PLACES XX ± .010 XXX ± .005	DRAWN C. ESTRADA	6-9-83
ANGLES ±0°30'	CHECK	
HOLES +.004 −.001	ENGINEER	
DO NOT SCALE DWG	ENGR APPR	
	Q A APPR	
	MFG APPR	

WESTERN DIGITAL CORPORATION

TITLE: WD1000-TB1

CLASS CODE	BASE NUMBER	DASH	BIN/ROM CODE	REV	DCLC
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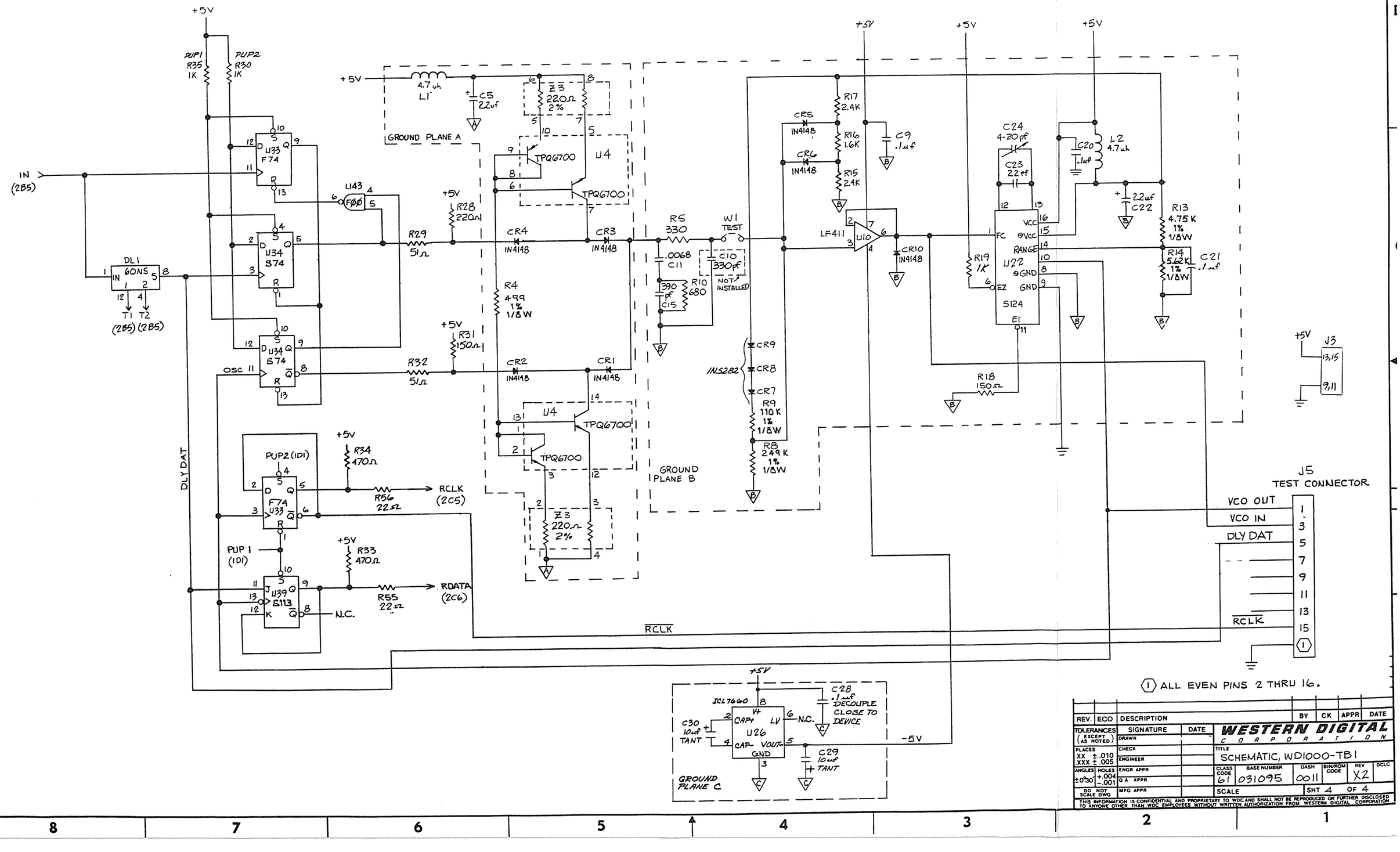
SCALE —— SHT 3 OF 4



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ANGLES ±0°30'	CHECK	
HOLES ± .004 − .001	ENGINEER	
DO NOT SCALE DWG	ENGR APPR	
	Q A APPR	
	MFG APPR	

WESTERN DIGITAL CORPORATION

TITLE: SCHEMATIC, WD1000-TB1

CLASS CODE	BASE NUMBER	DASH	BIN/ROM CODE	REV	DCLC
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SCALE | SHT 4 OF 4

REVISED													
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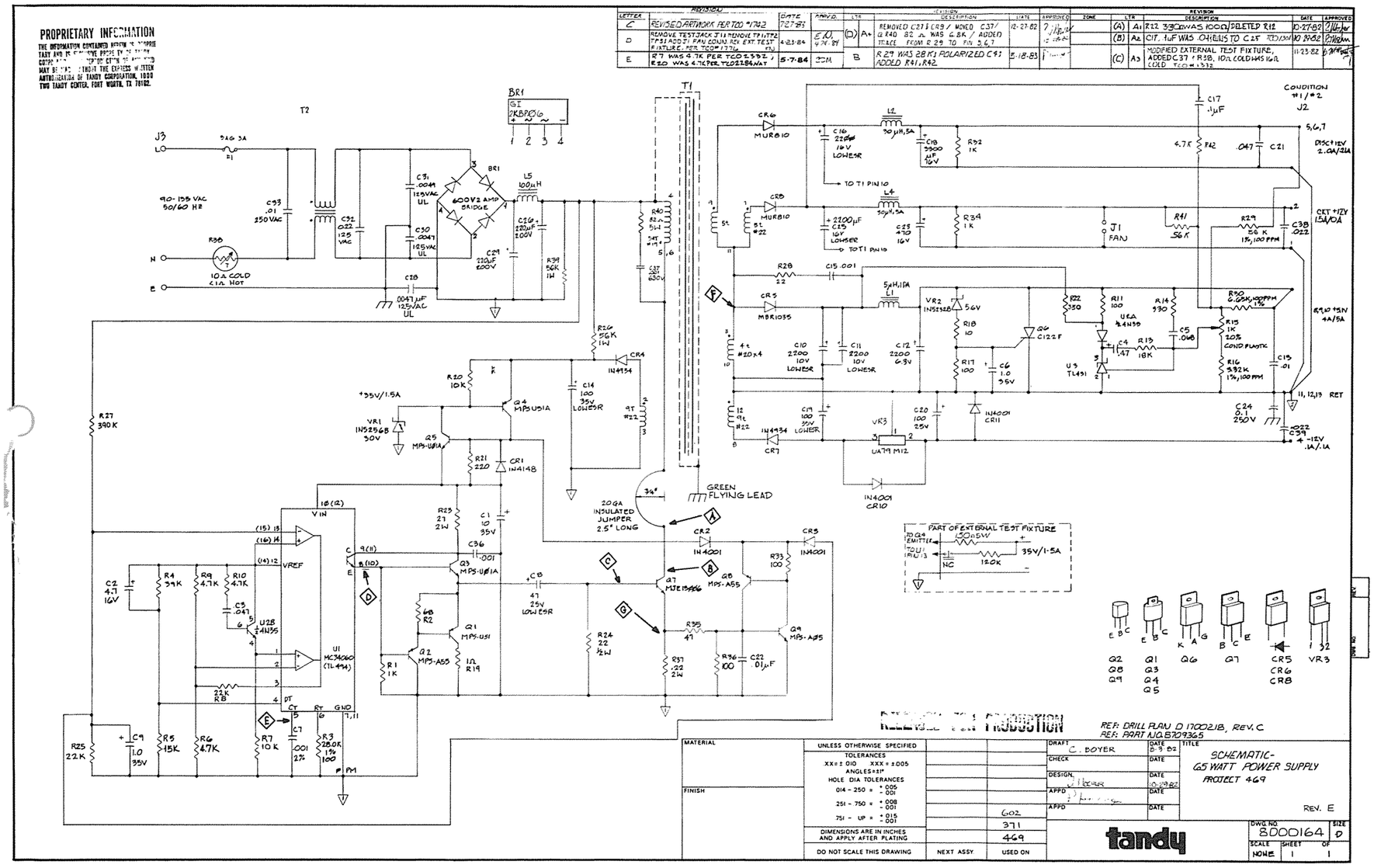
C	REVISED ARTWORK PER TCO #1742	7-27-83		(D)	A+ REMOVED C27 & CR9 / MOVED C37 / Q R40 82 Ω WAS 6.8K / ADDED TRACE FROM R 29 TO PIN 5,6,7	12-27-82			(A)	A1 R22 330Ω WAS 1000Ω / DELETED R18	10-27-82	
D	REMOVE TEST JACK J13 REMOVE TP1 TP2 TP3 ADD J7 FAN COUNT REV EXT. TEST FIXTURE PER TCO#1776	4-23-84							(B)	A2 CIT. 1uF WAS CHANGE TO C25 PER TCO#1809	10-30-82	
E	R7 WAS 4.7K PER TCO 2382 / R20 WAS 4.7K PER TCO 2284 WAT	5-7-84		B	R 29 WAS 28 K1 POLARIZED C91 ADDED R41, R42	5-18-83			(C)	A3 MODIFIED EXTERNAL TEST FIXTURE, ADDED C37 / R38, 10Ω COLD WAS 16Ω COLD TCO#1532	11-23-82	



MATERIAL	UNLESS OTHERWISE SPECIFIED TOLERANCES XX = ± .010 XXX = ± .005 ANGLES = ± 1° HOLE DIA TOLERANCES .014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001		
FINISH	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING	602	
	DO NOT SCALE THIS DRAWING	NEXT ASSY	371 469 USED ON

RELEASED FOR PRODUCTION
REF: DRILL PLAN D 17002JB, REV. C
REF: PART NO. B709365

DRAFT	C. BOYER	DATE	8-5-82
CHECK		DATE	
DESIGN		DATE	10-29-82
APPD		DATE	
APPD		DATE	

TITLE: SCHEMATIC- G5 WATT POWER SUPPLY PROJECT 469

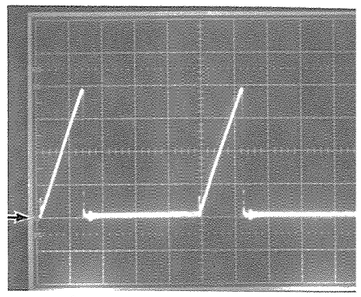
REV. E

tandy

DWG NO. 8000164 SIZE D
SCALE NONE SHEET 1 OF 1

WAVEFORMS

See schematic notations.
→ = 0 reference



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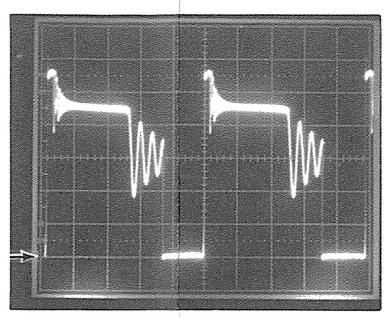
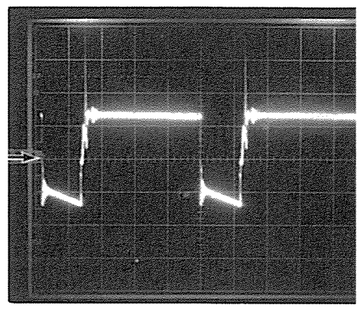
5 μ/d horiz. AC



Ⓑ 50 v/d vert.
5 μ/d horiz. DC



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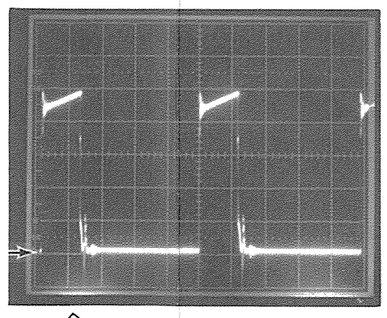

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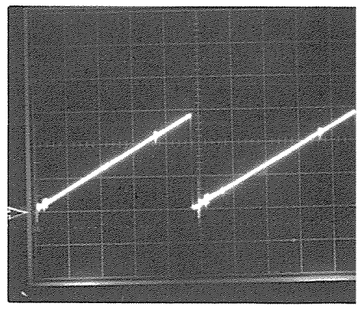

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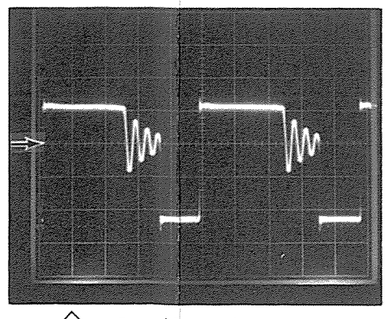

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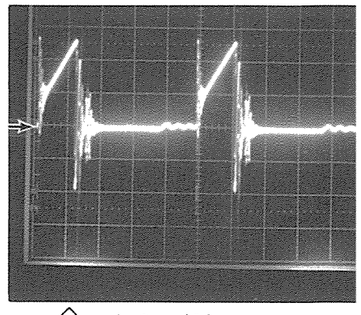
5 μs/d horiz. DC



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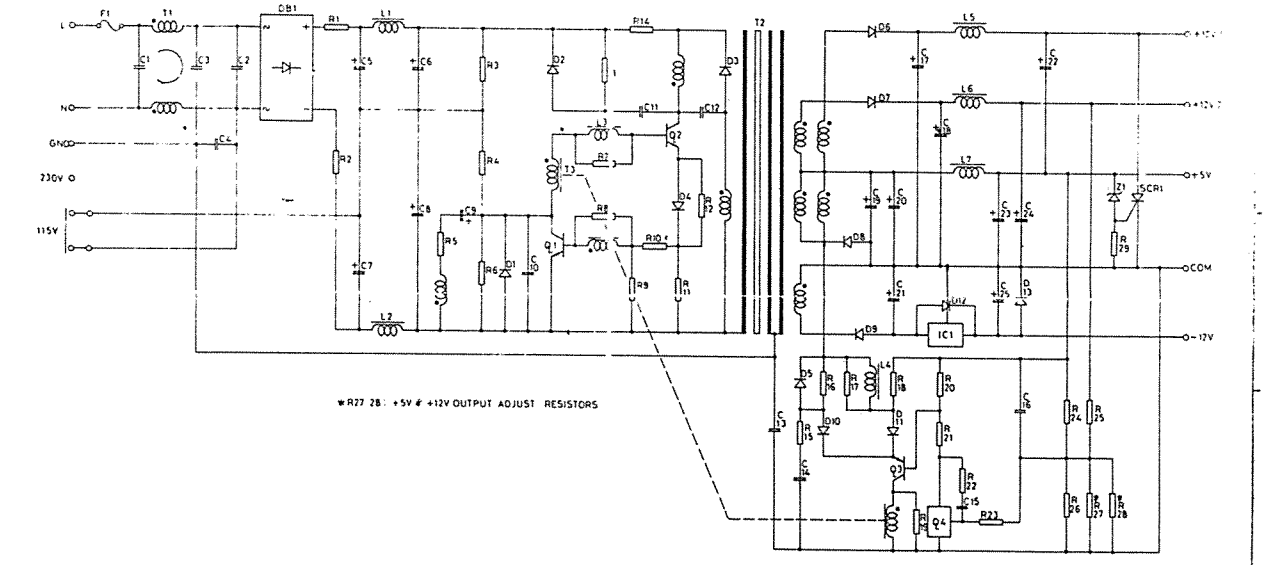

*R27 28 : +5V & +12V OUTPUT ADJUST RESISTORS

ASTEC 38W POWER SUPPLY

ISSUE	REVISIONS	APPD	CHK	DATE	ECN
1	REL. DRAWING			5.5.82	

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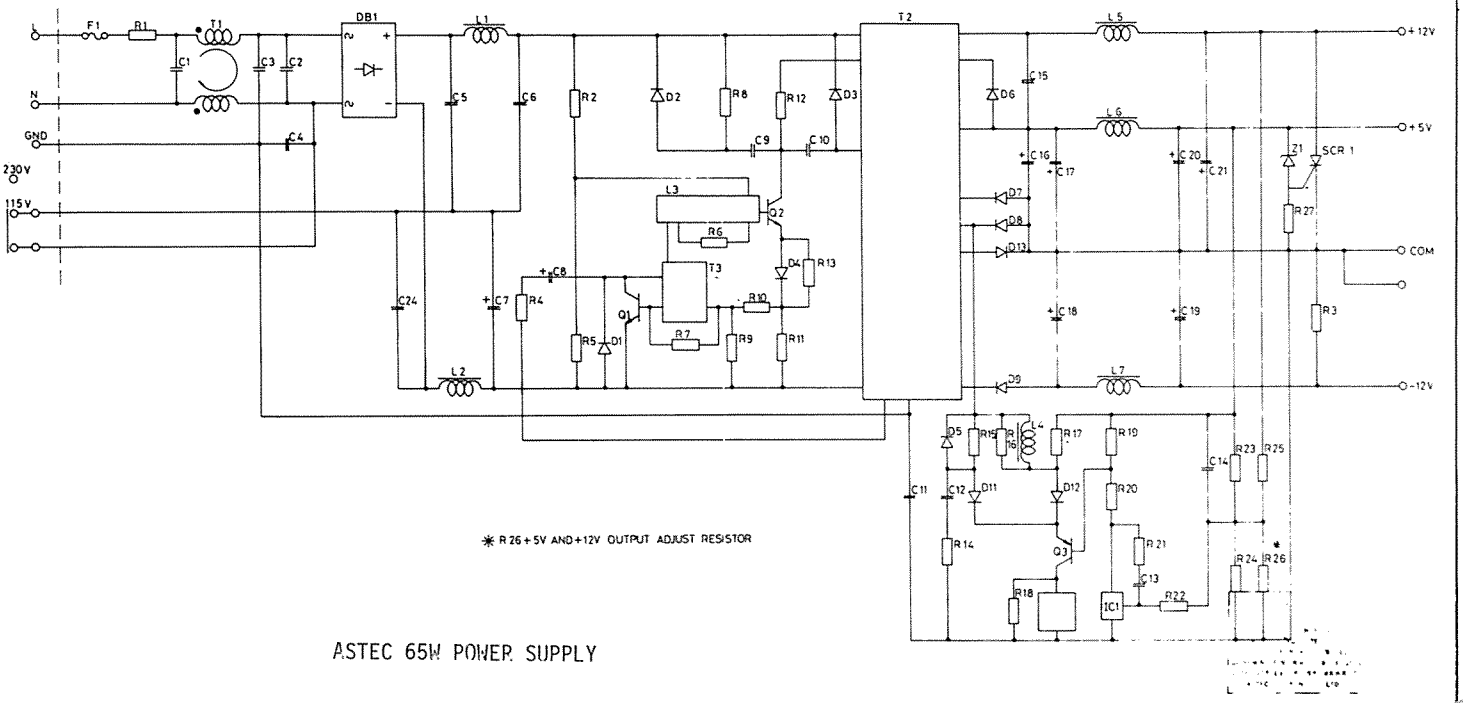
	DRG Y. F. CHAN 5.5.82	FIRST USED ON AA 12090 / PART NO
	CHK 5ma/82	MATERIAL / FINISH
	APPD 5/5/82	
ASTEC HONG KONG		SH 1 OF 1 A2



✳ R 26 + 5V AND +12V OUTPUT ADJUST RESISTOR

ASTEC 65W POWER SUPPLY

ISSUE	REVISIONS	DATE	CHK	APPD	ECN
1	RELEASE DRAW	11SEP80			

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN MM TOLERANCES WHOLE NO ± ANGLE ± DECIMAL x.x ± xx ±	DO NOT SCALE DRAWING	TITLE CIRCUIT DIAGRAM
	DRN ANDY LEUNG DATE 11SEP80	
	CHK DATE	FIRST USED ON P.A. 3330 / PART NO
	DATE 11SEP80	MATERIAL / FINISH
ASTEC COMPONENT LTD. HONG KONG		SH 1 OF 1 A2

12/15 Meg Hard Disk

Service Manual

TRS-80®

Radio Shack®

14/ Appendices:

The following documents are applicable to the 12/15 Meg Hard Disk Service Manual:

Tandon Corporation OEM Operating and Service Manual
Publication No. 179Ø45-ØØ1A (T5ØØ3 A 2-83)

Tandon Corporation OEM Operating and Service Manual
Publication No. 187275-ØØ4 (Rev C)

Tandy Corporation Service Manual
65 Watt Switching Power Supply #879ØØ49
Publication No. MS26Ø113ØJ-183

15/ Supplement

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2Ø32Ø Prairie Street
Chatworth, CA 91311

TANDON OEM OPERATING AND SERVICE MANUAL

MODEL NUMBERS TM6Ø2S, TM6Ø3S, AND TM6Ø3SE

5.25" RIGID DISK DRIVES

SEPTEMBER 2Ø, 1982

PRELIMINARY

TANDON CORPORATION
2Ø32Ø PRAIRIE STREET
CHATSWORTH, CA 91311

TEL. NO.: (213) 993-6644
TWX NO.: 91Ø-494-1721
TELEX NO.: 194794

TANDON INTERNATIONAL GMBH
AM SUEDPARK 7A
D-6Ø92 KELSTERBACH, WEST GERMANY

TEL. NO.: Ø6 11/49 61Ø7 2Ø91
TELEX NO.: 411547

P/N 187275-ØØ4 Rev. C

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LIST OF ILLUSTRATIONS

FIGURES

TABLES

APPENDIX

SECTION I--GENERAL INFORMATION

1.1 SCOPE

This manual contains information useful in the installation and operation of Tandon Corporation's TM600 family of 5.25" rigid disk drives. This manual also contains interface requirements and descriptions of signals. TM600 refers to Model Numbers TM602S, TM603S, and TM603SE, as appropriate.

1.2 INTRODUCTION

The TM600 family of 5.25" rigid disk drives are low-cost, random access memories that use moving head, noncontact recording techniques. There are both two- and three-platter models, which use standard Winchester technology and 130 millimeter rigid media.

This drive consists of storage media that is contained within the drive in a fixed (nonoperator removable) configuration, read/write and control electronics, the drive mechanism, a read/write head, a precision split band positioning device, and an air filtration system.

Interface flexibility is provided by using an industry standard interface on the drive. The "S" version is compatible with larger capacity disk drives. Compatible is defined as using the same pin assignment where the signal and the function are common.

1.3 DISK DRIVE PERFORMANCE CHARACTERISTICS

The information contained in Table 1 pertains to all models of the Tandon TM600 family of disk drives.

1.4 DISK DRIVE MODEL SPECIFICATIONS

Table 2 contains a list of the drive models available and the number of platters each one has.

Table 1

Disk Drive Performance Characteristics

Model	TM602S	TM603S	TM603SE
Disks/Platters	2	3	3
Heads/Recording Surfaces	4	6	6
TPI	254 TPI		
Cylinders	153	153	230
RPM	3600 RPM ± 1 percent		
Recording Capacity, Unformatted:			
Per Drive	6.38 MBytes	9.57 MBytes	14.35 MBytes
Per Surface	1.59 MBytes	1.59 MBytes	2.39 MBytes
Per Track	10.40 KBytes		
Transfer Rate	5 Mbits per second		
Recording Density (BPI)	7690	7690	9625
Tracks	612	918	1380
Access Time			
Track-to-Track	3 milliseconds		
Average	153 ms, 99 ms ramped seek	153 ms, 99 ms ramped seek	210 ms, 137 ms ramped seek
Head Settling Time	15 milliseconds		
Average Latency	8.34 milliseconds		
Mechanical Dimensions			
Height	3.25 inch		
Width	5.75 inch		
Length	8.00 inch		
Error Rates			
Soft Read	$1X10^{10}$ bits		
Hard Read	$1X10^{12}$ bits		
Seek Errors	$1X10^{6}$ seeks		
Power			
+12V D. C. +/-	10% 1.5 amps tyical, 5 amps maximum for 10 seconds with no more than 5 millivolts PARD* (see Figure 1).		
+5V D. C. +/-	5% .8 amps typical with no more than 50 millivolts PARD*		
Environmental			
Ambient Temperature:	Operating: 16°C to 46°C (50°F to 115°F)		
	Nonoperating: -35.4°C to 60°C (-40°F to 140°F)		
Relative Humidity:	8% to 80%		
Maximum Wet Bulb Temperature:	26°C without condensation		

*Periodic and Random Deviation.

Specifications Subject To Change Without Notice.

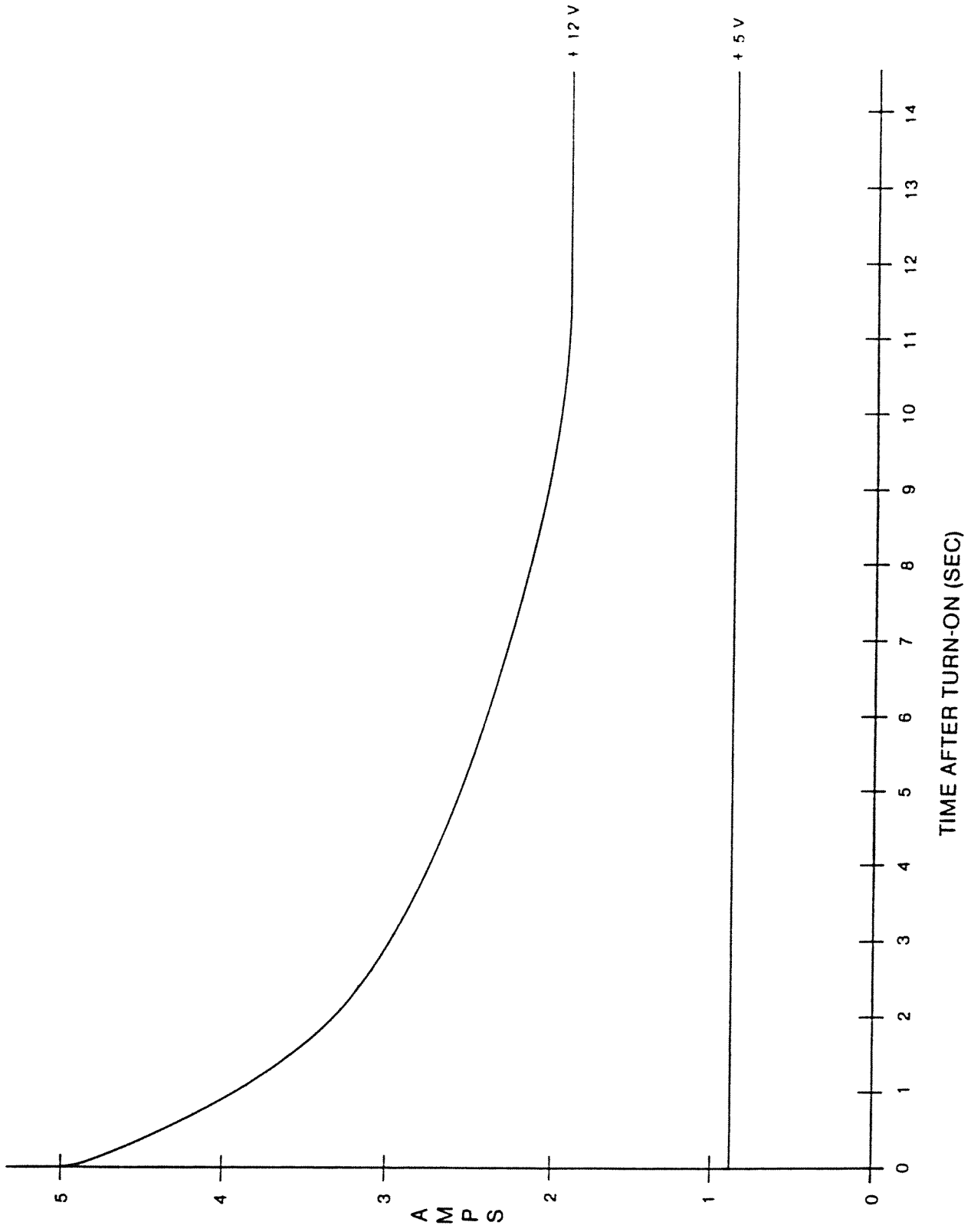


Figure 1
Typical Starting Currents At Nominal Voltage

Table 2

Disk Drive Model Specifications

Model Number	Number of Platters	Kind of Interface
TM602-S	2	Standard
TM603-SE	3	Standard/Extended Version
TM603-S	3	Standard

1.5 PHYSICAL DIMENSIONS

The major physical dimensions of the TM600 family of drives are contained in Figure 2. These dimensions are given in English and in metric units.

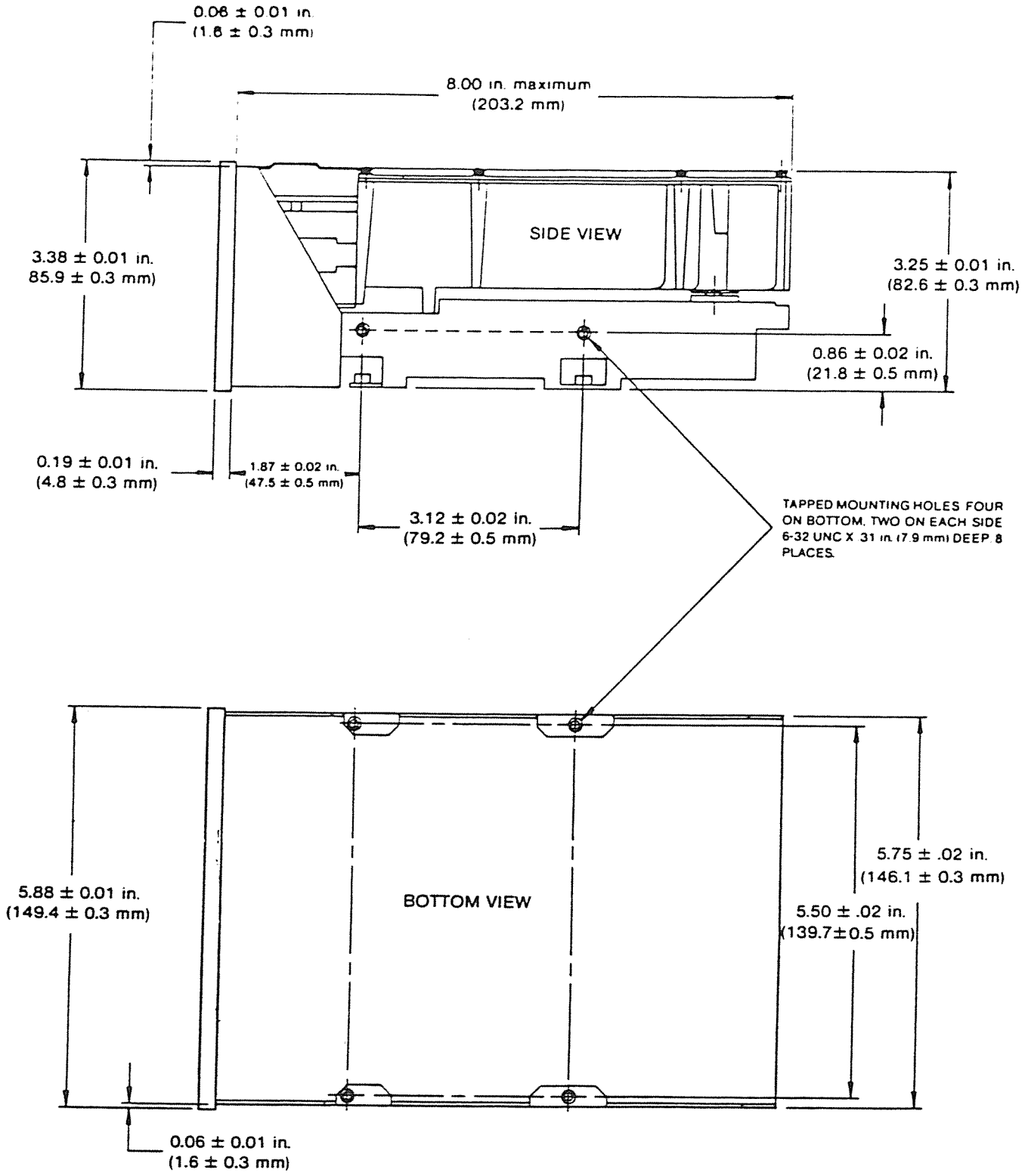


Figure 2

Disk Drive Physical Dimensions

SECTION II--INSPECTION, INSTALLATION, AND INTERFACES

2.1 INTRODUCTION

This section contains information pertinent to the inspection, installation, and interfaces of the Tandon TM600 family of rigid disk drives.

The electrical interface between the drive and the host system is via four connectors. J1 provides control signals for the drive. J2 provides for the radial connection of read/write data signals. J3 provides for D. C. power. J4 provides for frame ground. Figure 3 contains the locations of the interface connectors.

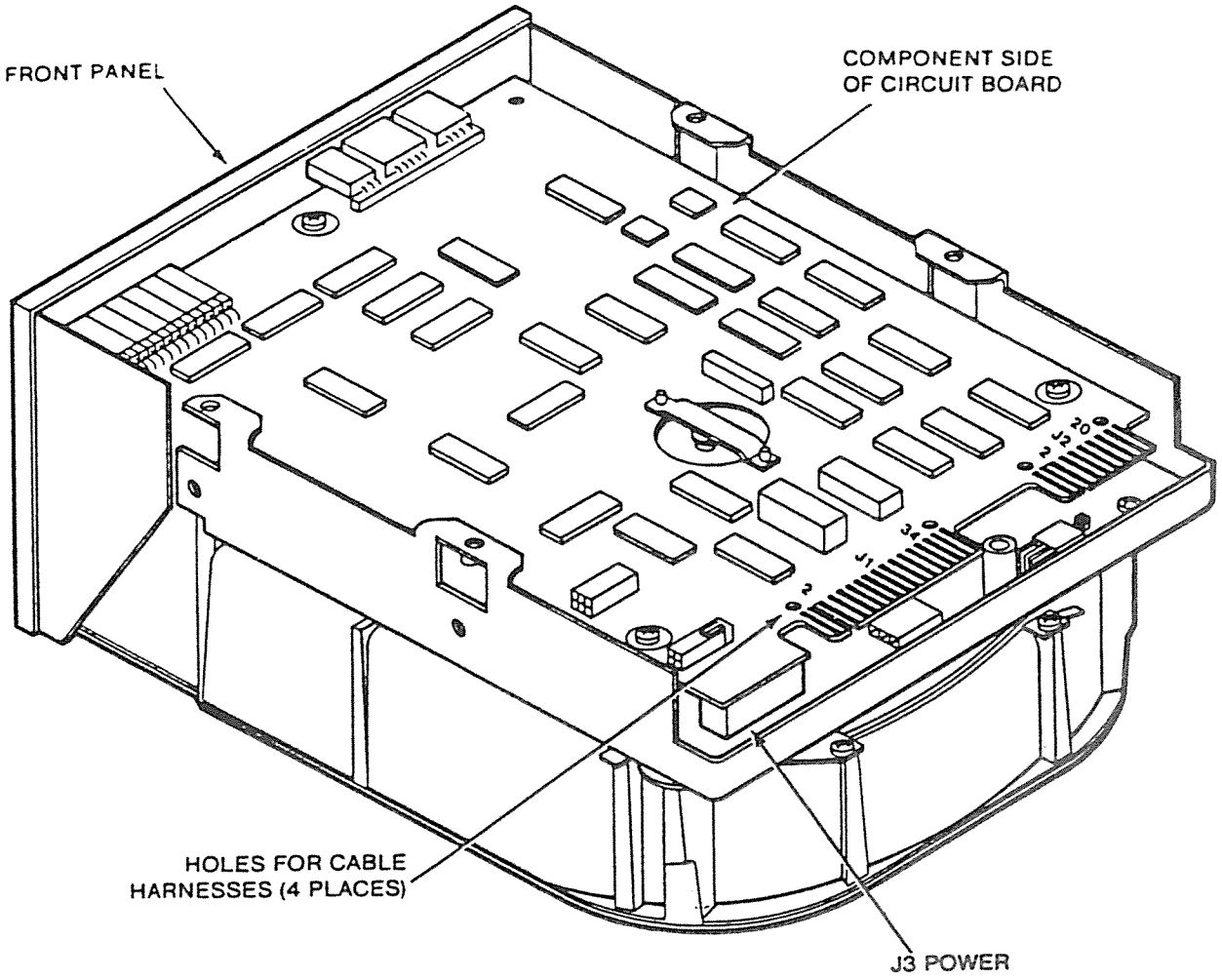
2.2 UNPACKING AND INSPECTION

The drive is shipped in a protective container which, when bulk packaged, minimizes the possibility of damage during shipment. The following procedure is the recommended method of uncrating the drive.

1. Place the shipping container on a flat work surface.
2. Remove the upper half of the inner container.
3. Remove the drive from the lower half of the inner container.
4. Check the model number and top assembly description against the packing slip.
5. Visually examine the contents of the shipping container for possible damage.
6. Notify the carrier immediately if any damage is found.
7. The inside chamber of the drive is a sealed compartment that must not be opened.

NOTE

REMOVAL OF THE COVER OF THE DRIVE INVALIDATES THE WARRANTY.



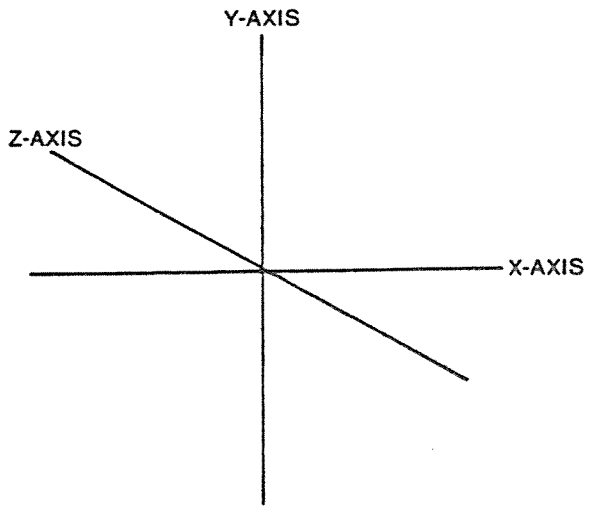


Figure 3

Locations of Interface Connectors

Before applying power to the disk drive, the following inspection procedure should be performed:

1. Check to ensure that the circuit boards are secure.

2. Check to ensure that the connectors are firmly seated.

3. Notify the carrier immediately if you find any damage.

2.3 MOUNTING CHARACTERISTICS

The mounting characteristics of the TM600 family of disk drives are contained in Figure 2. There are four 6-32, tapped mounting holes on the bottom of the disk drive, and two on each side of it.

2.4 POWER CABLING

The D.C. power connector, J3, is a four-pin AMP Mate-N-Lok device, P/N 350211-1, which is mounted on the solder side of the circuit board. The recommended mating connector, P3, is AMP P/N 1-480424-0, using AMP pins P/N 60617-4. J3 pins are labeled on the J3 connector. Figure 4 contains an illustration of the J3 connector.

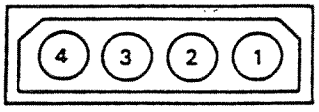


Figure 4

J3 Connector

The frame ground connector, J4 is the Faston AMP P/N 61761-2. The recommended mating connector is AMP P/N 62187-1.

2.5 STANDARD INTERFACE

The standard or "S" model interface is contained in Table 2-1. Connection to J1 is via a 34-pin circuit board edge connector. The dimensions of the J1 connector are found in Figure 5. The pins are numbered 1 through 34. The even numbered pins are located on the compoenent side of the circuit board. Pin 2 located on the end of the circuit board connentor closest to the D. C. power connector J3/P3, and it is labeled. A key slot is located between Pins 4 and 6.

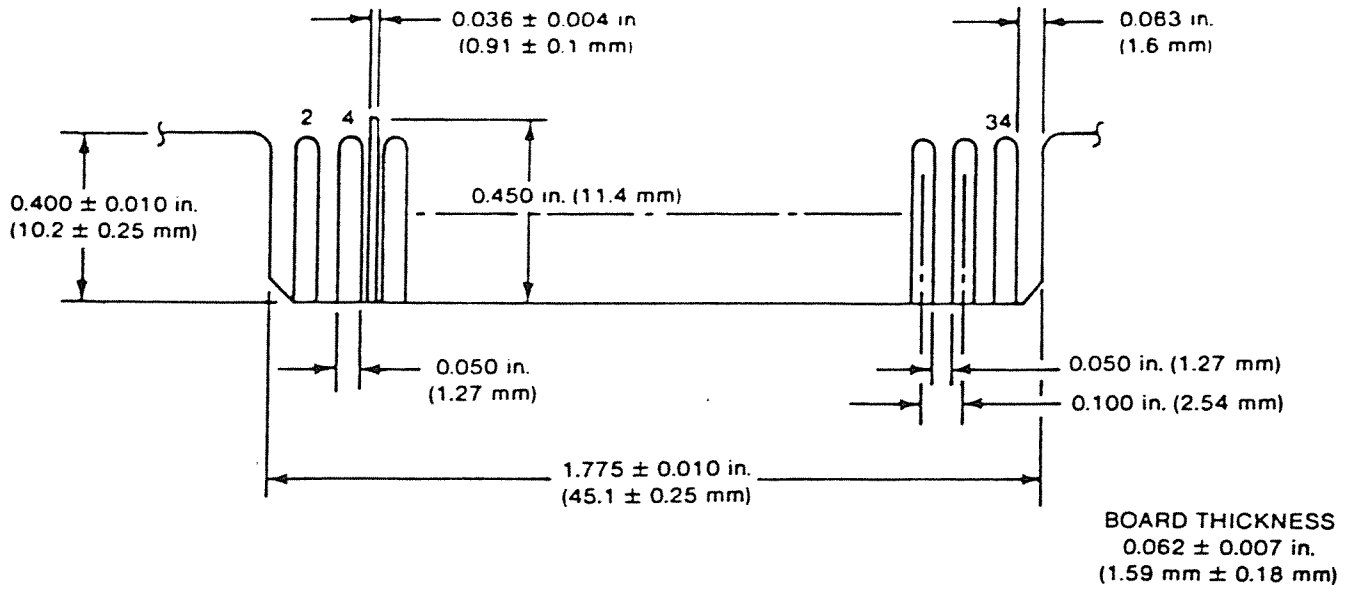


Figure 5
J1 Connector Dimensions

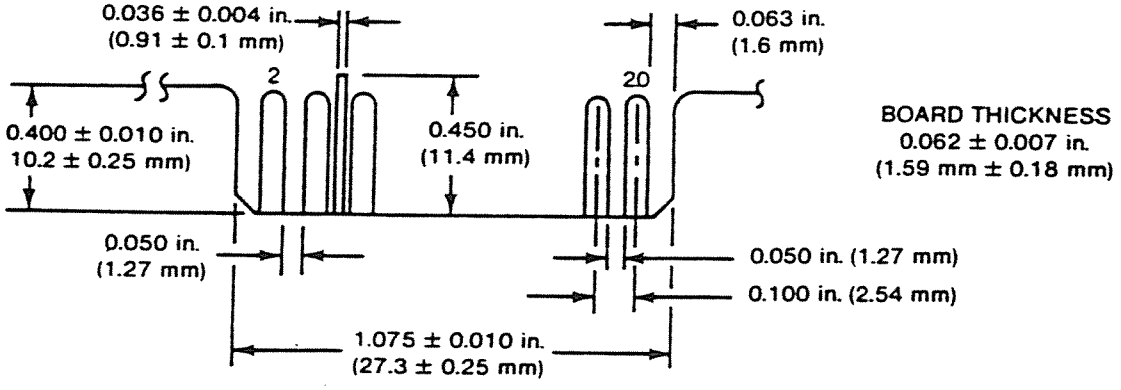


Figure 6

J2 Connector Dimensions

The recommended mating connector for P1 is a 3M ribbon connector, P/N 3463-0001, without ears.

Connection to J2 is via a 20-pin circuit board edge connector. The dimensions of the J2 connector are found in Figure 6. The pins are numbered 1 through 20. The even numbered pins are located on the component side of the circuit board. The recommended mating connector for P2 is a 3M ribbon connector, P/N 3461-0001, without ears. A key slot is located between Pins 4 and 6.

Table 3

Standard Interface

Connector	Interface Pin Number Signal	(Gnd)	Signal Type	I/O	Signal Name
P1 ^	2	(1)	S	I	Reduce Write I
|	4	(3)	S	-	Head Select 2^2
|	6	(5)	S	I	Write Gate
|	8	(7)	S	O	Seek Complete
|	10	(9)	S	O	Track 000
34-Pin	12	(11)	S	O	Fault
Ribbon	14	(13)	S	I	Head Select 2^0
Daisy	16	(15)	-	-	Reserved (To J2-7)
Chain	18	(17)	S	I	Head Select 2^1
|	20	(19)	S	O	Index
|	22	(21)	S	O	Ready
|	24	(23)	S	I	Step
|	26	(25)	S	I	Drive Select 0
|	28	(27)	S	I	Drive Select 1
|	30	(29)	S	I	Drive Select 2
|	32	(31)	S	I	Drive Select 3
P1 v	34	(33)	S	I	Direction In
P2 ^	1	(2)	S	O	Drive Selected
|	3	(4)	S	-	Reserved (+5 V)
|	5	(6)	S	I	Reset
|	7	(8)	-	-	Reserved (To J1-16)
20-Pin	9	(10)	-	-	Spare
Ribbon	11	(12)	-	-	Ground
Daisy	13		D	I	+ Write Data
Chain	14		D	I	- Write Data
or	15	(16)	-	-	Ground
Radial	17		D	O	+ Read Data
v	18		D	O	- Read Data
P2	19	(20)	-	-	Ground
P3 ^	1			-	+12 V D. C. In
4-Pin Power	2			-	12 V Return
Radial	3			-	5 V Return
P3 v	4			-	+5 V D. C. In

Notes:

1. S - Single ended
2. D - Differential
3. I - Drive input
4. 0 - Drive output

SECTION III--THEORY OF OPERATION

3.1 INTRODUCTION

There are three kinds of interface signals:

1. Input Control Lines
2. Output Control Lines
3. Data Transfer Lines

Signals on the Input Control lines are standard TTL levels. They have the following electrical specifications:

True: Ø.Ø volt D. C. to Ø.4 volt D. C. @ I = 4Ø mA maximum

False: 2.5 volt D. C. to 5.25 volt D. C. @ I = Ø mA open

See Figure 7 for the recommended circuit.

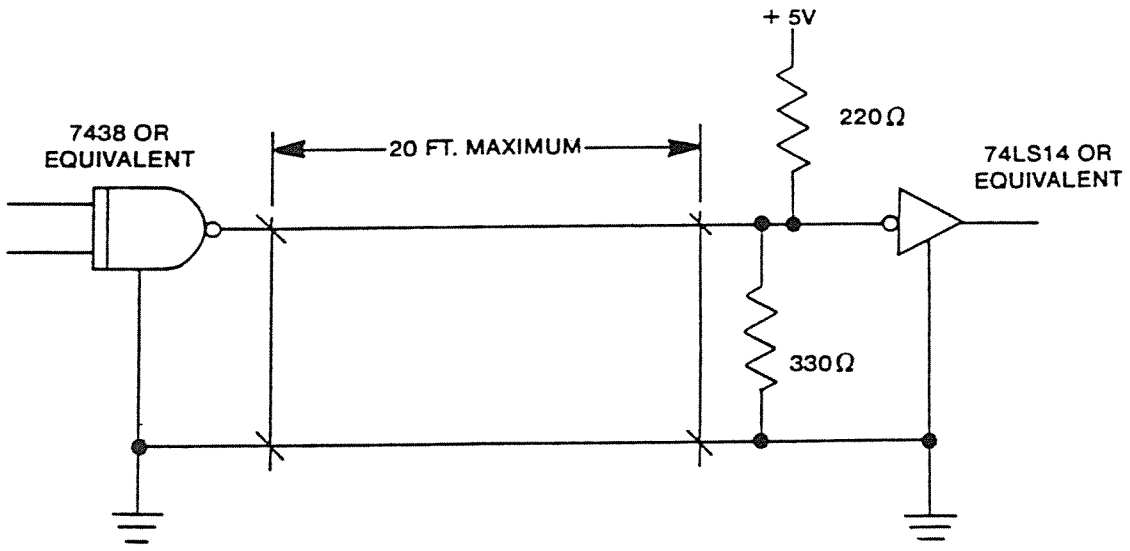


Figure 7

Control Signal Driver/Receiver Circuit Combination

3.2 INPUT CONTROL LINES

There are two kinds of Input Control lines, those that are multiplexed in a multiple drive system and those that do the multiplexing.

The Input Control lines that are multiplexed include:

1. Reduced Write Current
2. Write Gate
3. Head Select
4. Step Interface
5. Direction In

The Input Control lines that do the multiplexing are:

1. Drive Select Ø
2. Drive Select 1
3. Drive Select 2
4. Drive Select 3

3.2.1 Reduced Write Current

When this Input Control line is activated low (true) in conjunction with the write gate, a lower value of write current is selected for writing on the disk. When the signal is set high (false), the higher value write current is selected. When writing on Tracks Ø through 127, it is recommended that this line be set false. For Tracks 128 and greater, the Reduced Write Current line should be set true.

A 22Ø/23Ø ohm resistor pack allows the line to be terminated.

3.2.2 Write Gate

The Write Gate signal enables data to be written on the disk when it is activated or when the logical zero (true) level is reached. The ready line must be valid before write gate is activated. If a disk drive fault occurs, further writing on the disk is prohibited. In addition, the Seek Complete line should go true before you begin to write any information on the disk.

The inactive or logical high (false) level on the Write Gate line enables the step pulses to step the head arm actuator.

3.2.3 Head Select

There are three Head Select lines. They are used to select each read/write head--Ø, 1, or 2--in a binary coded sequence.

Head Select signals are logic low (true) levels. They must be activated in conjunction with the Drive Select lines. The heads are numbered Ø through 5. Head Select Ø is the least significant line. Table 3-1 contains information about the Head Select line sequence, disk drive model number, and numbers that may be selected.

Table 3-1

Head Select

Head Select Line Sequence			Model Number	
			TM6Ø2	TM6Ø3
2^2	2^1	$2^Ø$	Head Number	Selected
1	1	1	Ø	Ø
1	1	Ø	1	1
1	Ø	1	2	2
1	Ø	Ø	3	3
Ø	1	1		4
Ø	1	Ø		5

Legend: 1 = Logical High (False)
Ø = Logical Low (True)

A 22Ø/33Ø ohm resistor pack allows the line to be terminated.

3.2.4 Step Interface

When the Step Interface line is activated in conjunction with the Direction In line, the read/write heads move in the direction defined by the Direction In line. The motion is initiated by a logical zero to a logical one transition or by the trailing edge of the step pulse. Any change in the Direction In line must be made one hundred nanoseconds before the leading edge of the step pulse. The quiescent state of this line should be held logically high (false).

The heads move at the rate of the incoming step pulses. Figure 8 contains the sequence and the requirements for step timing.

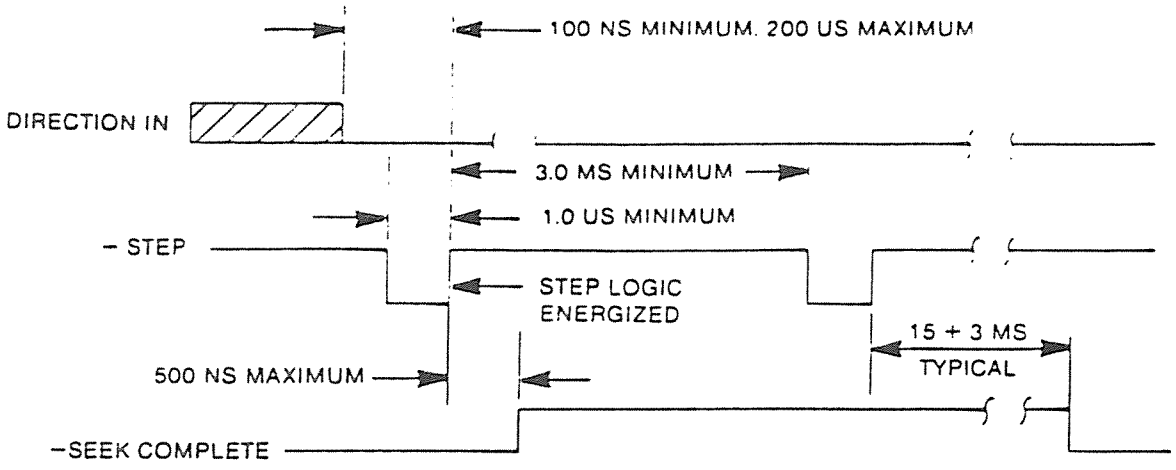


Figure 8

Step Mode Timing Diagram

3.2.5 Direction In

The Direction In line determines the motion of the read/write heads when a step pulse is issued. The motion is toward the center of the disk if the Direction In line is in the true (low) state when a step pulse occurs. The direction of the motion is away from the center of the disk if the Direction In line is in the false (high) state when a step pulse occurs.

A 220/330 ohm resistor pack allows the line to be terminated.

3.2.6 Drive Select

Drive Select lines Ø through 3 provide a means of selecting and deselecting a drive. These four lines select one of four drives that are daisy chained to the controller.

The drive address is determined by a select shunt on the Signal circuit board. Drive Select lines Ø through 3 provide a means of daisy changing a maximum of four drives to a controller.

When logically high (false), the output drivers are open circuits or logically high (false), and the drive receivers do not acknowledge signals presented to them. A Drive Select line must remain stable in the true (low) state until a Step or Read/Write command is executed.

Only one line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more Drive Select lines are in the true (low) state simultaneously.

3.3 OUTPUT CONTROL LINES

The Output Control lines are enabled by their respective Drive Select line. They send status information to the controller, such as: drive selected, seek complete, Track000 fault, and line ready. In addition, the Index line is provided as an output to the controller for timing information.

The Output Control lines use an open collector gate that is capable of sinking a maximum of forty milliamperes in a logical low (true) level, with a maximum voltage of 0.4 volt measured at the driver. When the gate is off or logically high (false), the collector cutoff is a maximum of 250 u amps. See Figure 8 for the recommended circuit.

3.3.1 Drive Selected

When the Drive Selected lines coincide with the selected jumper on the shunt pack, the Select Status line goes logically low (true). This line informs the host system of the selection status of the drive.

NOTE

ONLY ONE DRIVE MAY BE SELECTED AT A TIME.

3.3.2 Seek Complete

The Seek Complete line indicates that the read/write heads have settled on the selected track at the end of a seek sequence. This status line is set logically zero (true) at the end of a normal seek. It is set logically high (false) in two cases:

1. A recalibration sequence is initiated by drive logic at power on because the heads are not over Track 000.

2. Five hundred nanoseconds, typical, after the leading edge of a step pulse or of a series of step pulses.

3.3.3 Track 000

The Track 000 line indicates to the host system that the read/write heads are positioned on Track 000. The Track 000 line goes logically low (true) only when the heads are positioned on Track 000. It remains low until the heads are moved away from Track 000, the outermost data track.

3.3.4 Fault

The Fault line indicates to the host system that a condition exists on the disk drive that is going to cause improper writing on the disk. When this line is logically low (true), Write Data is inhibited and further writing on the disk is pro-hibited until the condition is corrected. The condition under which the Fault line goes true is that D.C. voltages are grossly out of tolerance.

3.3.5 Line Ready

In conjunction with the Seek Complete line, the Line Ready line indicates to the host system that the disk drive can read, write or seek, and that all I/O signals are valid. The Line Ready line goes logically low (true) approximately 15 seconds after power on. The Line Ready line goes logically high (false) if the drive is not selected or if the speed of the motor is too slow. When this line is false, all writing and seeking is inhibited.

3.3.6 Index

An index pulse is provided once every revolution (16.67 ms nominal) to indicate the beginning of a track to the con-troller. The transition from logically high (false) to logically low (true) is the only valid transition. The leading edge of the pulse must be used to ensure accurate timing.

3.4 DATA TRANSFER LINES

The Data Transfer lines transfer information between the host system and the disk drive when the drive is selected. These lines are differential in nature. They may be multiplexed when using Drive Select.

The MFM Write Data pair of lines and the MFM Read Data pair of lines are provided for the transfer of data. Figure 9 contains a typical driver/receiver circuit combination used for data transfer signals.

3.4.1 MFM Write Data

The MFM Write Data lines are the differential pair that provide the data to be stored on the track. A flux reversal on the track to be written is caused when the plus (+) MFM

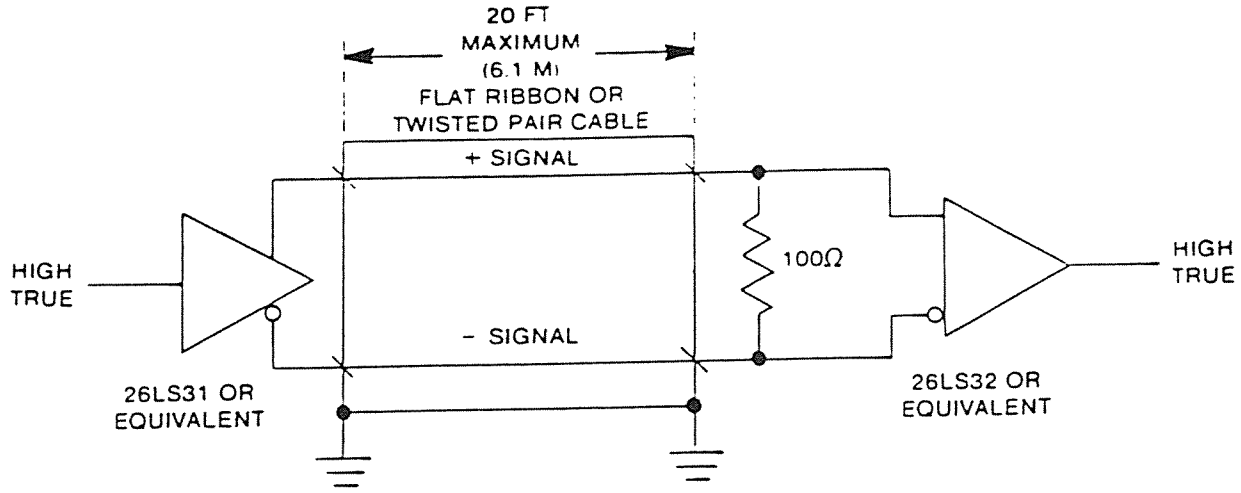


Figure 9

Data Line Driver/Receiver Circuit

Write Data line goes more positive than the minus (-) MFM Write Data line, provided that the Write Data line is logically low (true). When the disk drive is in a Read mode, the host system must ensure that the MFM write data signals are in the inactive state. The inactive state can be attained by making the plus MFM Write Data line more negative than the minus MFM Write Data line.

3.4.2 MFM Read Data

These lines are a differential pair that recover the data previously written on a track. A flux reversal on the track to be read is caused when the plus MFM Read Data line goes more positive than the minus MFM Read Data line. Subsequently, the differential pair signal is transmitted to the host system via the MFM Read Data lines.

APPENDIX A

CUSTOMER INFORMATION BULLETINS

CUSTOMER INFORMATION BULLETIN

TM600 RIGID DISK DRIVE

RAMPED SEEK MODE

Tandon uses a Customer Information Bulletin to inform our customers of changes in and improvements to our products. The following information is an option on the Tandon TM600 family of rigid disk drives that may be of interest in your application.

Our current drives are designed to operate at a minimum time between steps of three (3) milliseconds. Given eighteen (18) milliseconds for last step and settling time, this step rate results in an average seek time of 170 milliseconds for the 153 cylinder drive.

Customer requirements may necessitate a reduction in average seek time. By using the ramped seek mode and giving correct step pulse timing, the present drive's average access time can be improved.

A. In order to use a ramped seek, four major conditions must be met:

1. The drive must have a Control and Data circuit board, P/N 187045-001.

2. The Pins 8 and 9 programming shunt of the Control and Data circuit board must be closed (shorted).

3. The viscous damper must be mounted to the stepper motor.

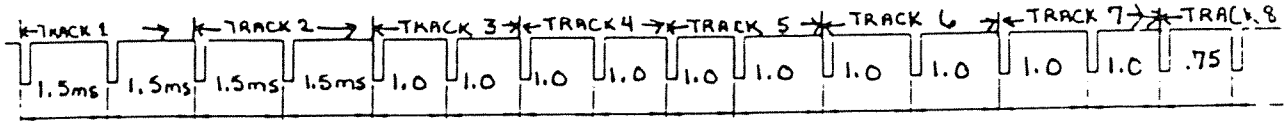
4. The controller must issue step pulses in accordance with the algorithm below. Note that two pulses per track are required in ramped seek.

B. The pulse timing for single-track to nine-track seek is:

Two pulses separated by 1.5 milliseconds for each track, i.e., a one-track seek is equal to two pulses, a nine-track seek is equal to fourteen pulses.

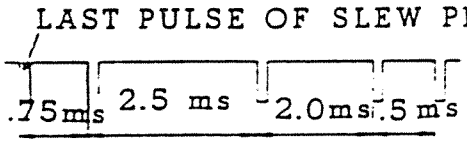
C. Pulse timing for an 10 track seek or greater.

1. Acceleration Phase:



2. Slew Phase: two pulses separated by .75 milliseconds for each track.

3. Deceleration Phase: last two tracks or seek.



If you have any questions or need additional information, please do not hesitate to contact me.

APPENDIX B

SCHEMATICS

NOTE

THE FOLLOWING VALUES WILL DIFFER DEPENDING ON WHICH UNIT, THE OXIDE MEDIA OR THE PLATED MEDIA, THE REPAIR TECHNICIAN IS SERVICING.

-ØØ1 = OXIDE MEDIA
-1Ø1 = PLATED MEDIA

FOR THE -ØØ1 OXIDE MEDIA R55 WILL BE A VALUE OF 62Ø OHMS.
FOR THE -1Ø1 PLATED MEDIS R55 WILL BE A VALUE OF 51Ø OHMS.

FOR THE -ØØ1 OXIDE MEDIA R87 WILL BE A VALUE OF 1ØØ OHMS.
FOR THE -1Ø1 PLATED MEDIA R87 WILL BE A VALUE OF 18Ø OHMS.

FOR THE -ØØ1 OXIDE MEDIA C54 WILL BE A VALUE OF 47 PFD.
FOR THE -1Ø1 PLATED MEDIA C54 WILL BE DELETED.

All TM500's have a top bill number on the back of the drive, which will identify type of drive. Also, the PCBA has a different part number.

187345-001	Oxide Media only.
187345-101	Hard Coat Platted only.

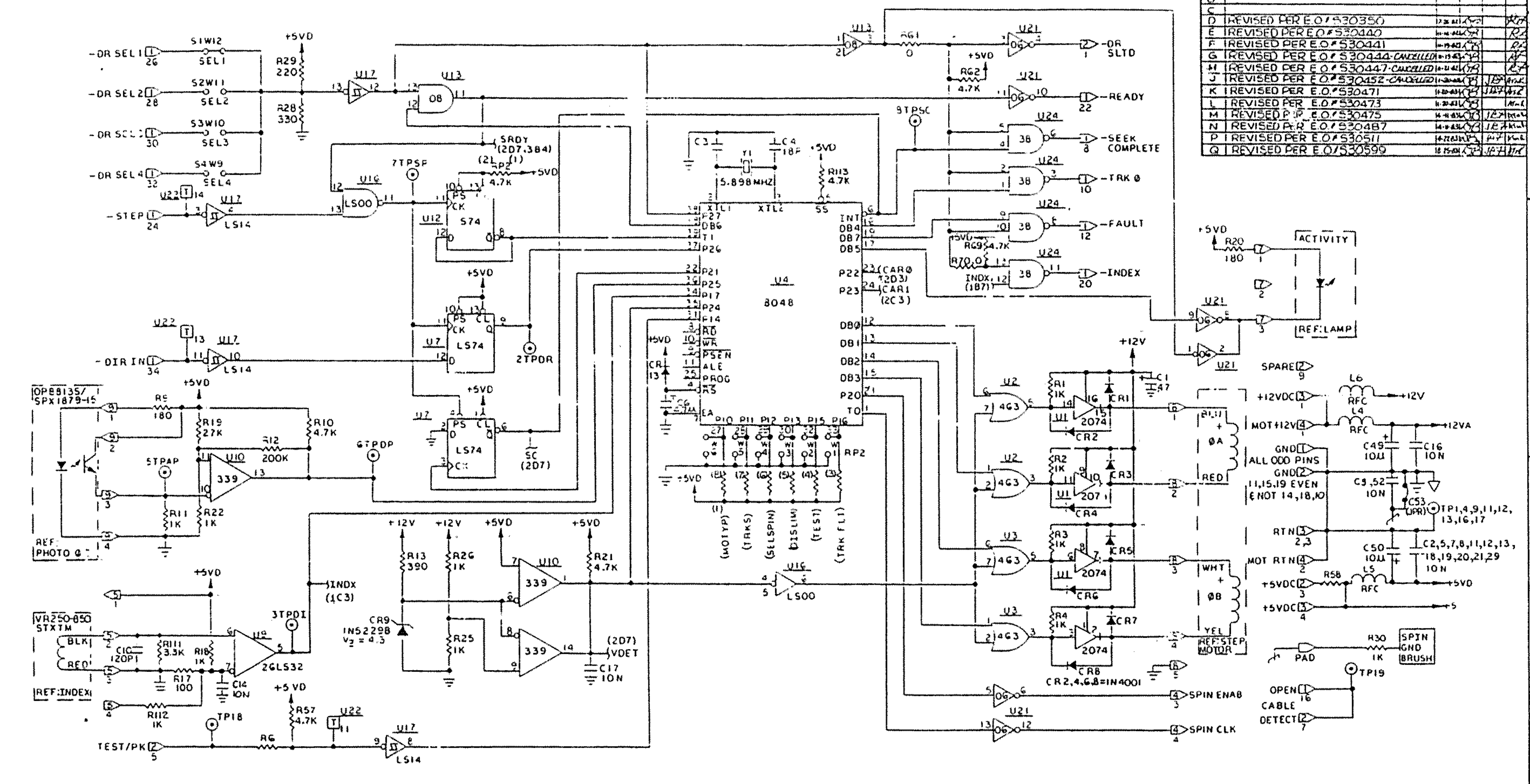
TM502

Top Bill Number	PCBA Number
187500-225	187345-001
-220	"
-224	"
187500-520	187345-101
-525	"
-825	"

TM503

Top Bill Number	PCBA Number
187500-321	187345-001
-322	"
-326	"
187500-921	187345-101
-926	"

REV	DESCRIPTION	DATE	DR	CHK	APPR
B					
C					
D	REVISED PER E.O#530350	[illegible]	[illegible]		[illegible]
E	REVISED PER E.O#530440	[illegible]	[illegible]		[illegible]
F	REVISED PER E.O#530441	[illegible]	[illegible]		[illegible]
G	REVISED PER E.O#530444-CANCELLED	[illegible]	[illegible]		[illegible]
H	REVISED PER E.O#530447-CANCELLED	[illegible]	[illegible]		[illegible]
J	REVISED PER E.O#530452-CANCELLED	[illegible]	[illegible]	[illegible]	[illegible]
K	REVISED PER E.O#530471	[illegible]	[illegible]	[illegible]	[illegible]
L	REVISED PER E.O#530473	[illegible]	[illegible]		[illegible]
M	REVISED PER E.O#530475	[illegible]	[illegible]	[illegible]	[illegible]
N	REVISED PER E.O#530487	[illegible]	[illegible]	[illegible]	[illegible]
P	REVISED PER E.O#530511	[illegible]	[illegible]	[illegible]	[illegible]
Q	REVISED PER E.O#530599	[illegible]	[illegible]	[illegible]	[illegible]



6. [X] Y DENOTES CONNECTOR JX, PIN Y.
5. INDUCTORS ARE IN μH, 10%.
4. DIODES ARE IN4446 OR EQUIV.
3. CAPS ARE IN PF, NF, OR μF. 25V MIN. TOLERANCE IS 10% FOR VALUES ABOVE 1N, 5% OTHERWISE.
2. 1% RESISTORS ARE 1/8W.
1. RESISTORS ARE IN OHMS, 1/4 W 5%.
NOTES: UNLESS OTHERWISE SPECIFIED

9. UNVALUED COMPONENTS ARE OMITTED.
8. [T]x DENOTES PIN X OF (U22) TERM PAK = 220 330
7. DENOTES TEST POINT.

Tandon CORPORATION

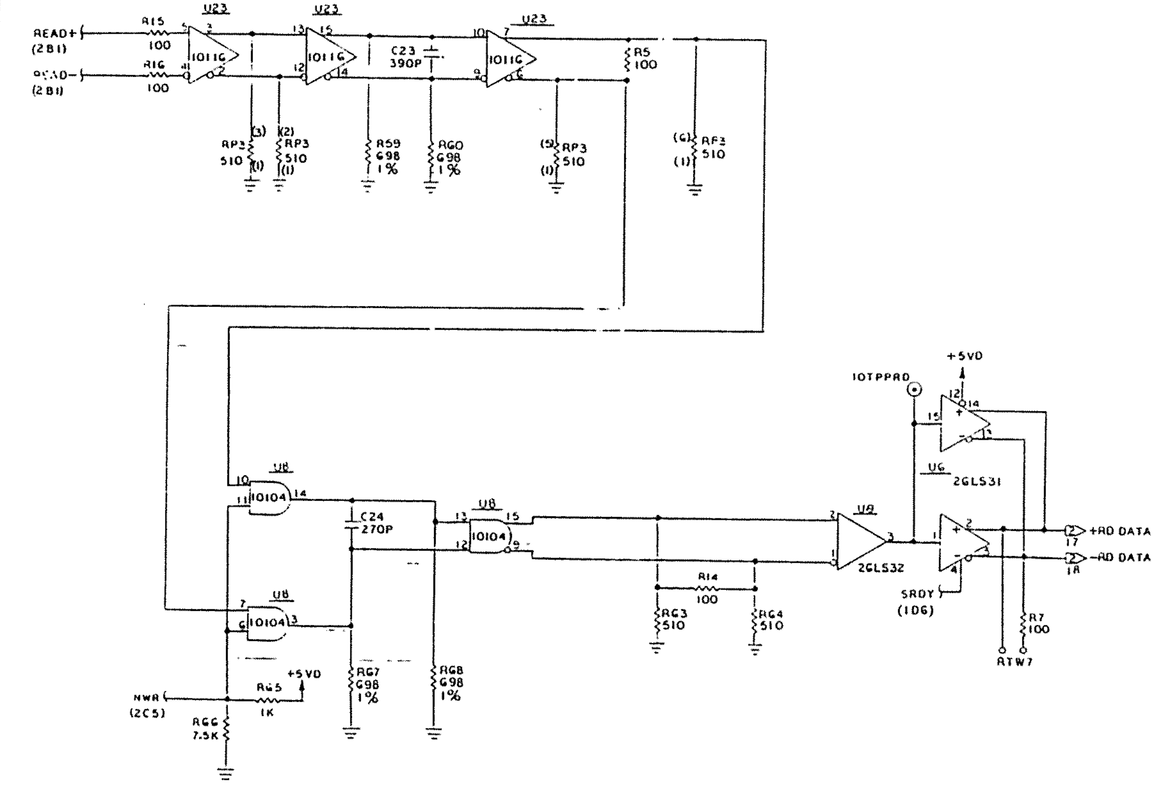
TITLE: CIRCUIT SCHEMATIC TM600 MAIN — μP

SIZE: D | DWG NO: 187340-001 | REV: Q

187340-001 | TM 600
CIRCUIT SCHEMATIC

3 of 3

REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				



I.C. LOCATION AND VOLTAGE CHART					
LOCATION	TYPE	+5	+12	GND	UNUSED
U16	74LS00	14		7	
U21	7406	14		7	
U11	7407	14		7	
U13	7408	14		7	
U17	74LS14	14		7	1/6
U24	7438	14		7	
U18, U15	7445	16		8	
U7	74LS74	14		7	
U12	74S74	14		7	
U10	339		3	12	1/4
U2, U3	463	8		4	
U30, U32	592		NOTED	NOTED	
U1	UNL2074		NOTED	4,5,12,13	
U6	26LS31	16		8	2/4
U9	26LS32	16		8	1/4
U25, U29	2719				
U20	Q2T2905		NOTED		1/4
U4	8048	26,40		20	
U8	10104	1,16		8	1/4
U23	10116	1,16		3	
U14					
U22	TERM PAK	16		7,8	4/12

SHUNT PLUG PROGRAMMING			
W1-W13 SHUNT	FUNCTION	FACTORY PROGRAMMED	USAGE
W1	TRK FAULT	O	INSTALL FOR EXCESS TRK FAULT
W2	TEST	O	INSTALL FOR FACTORY TEST
W3	DISABLE LIMIT	O	INSTALL TO DISABLE SOFT LIMITS
W4	SPIN SELECT	O	INSTALL FOR SPIN SELECT
W5	TRACKS	S	INSTALL FOR S VERSION ONLY
W6	MOTOR TYPE	–	INSTALL FOR TYPE 18 MOTOR
RTW7	READ TERMINATOR	I	CLOSE ONLY @ END DRIVE OF DAISY CHAIN DATA
WTW8	WRITE TERMINATOR	I	CLOSED FOR RADIAL DATA
S4W9	DRIVE SELECT 4	O	INSTALL 1 OF 4 PLUGS ONLY
S3W10	DRIVE SELECT 3	O	PLUG CORRESPONDS TO
S2W11	DRIVE SELECT 2	O	DRIVE ADDRESS
S1W12	DRIVE SELECT 1	I	
3PW13	3 DISC	603	CLOSE FOR MODEL 603 ONLY
U22	TERMINATOR PAK	I	INSTALL IN END DRIVE OF DAISY CHAIN

O = OMIT
I = INSTALL
S = CLOSE FOR S VERSION ONLY
603 = CLOSE FOR TM603 ONLY

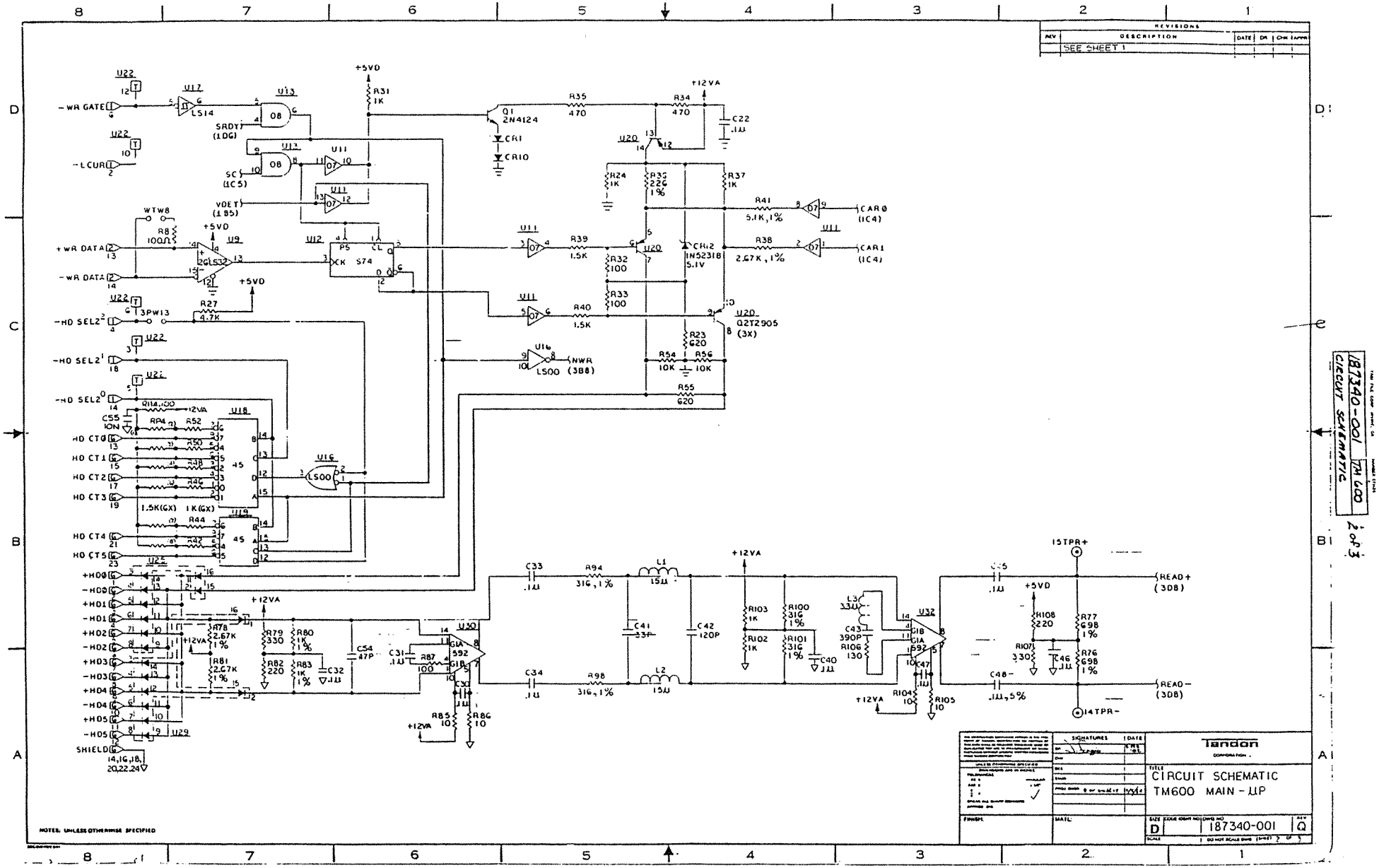
REFERENCE DESIGNATORS	
LAST USED	UNUSED
C54	C15,25-28,35-39,44,51
CR13	
J9	
L5	
Q1	
R113	R71 THRU 75,84,88,93,95-97,99,109,110
RP3	RP1, RP4 (PINS)
TP19	
U32	U5,14,15,26-28,31
W13	
T1	

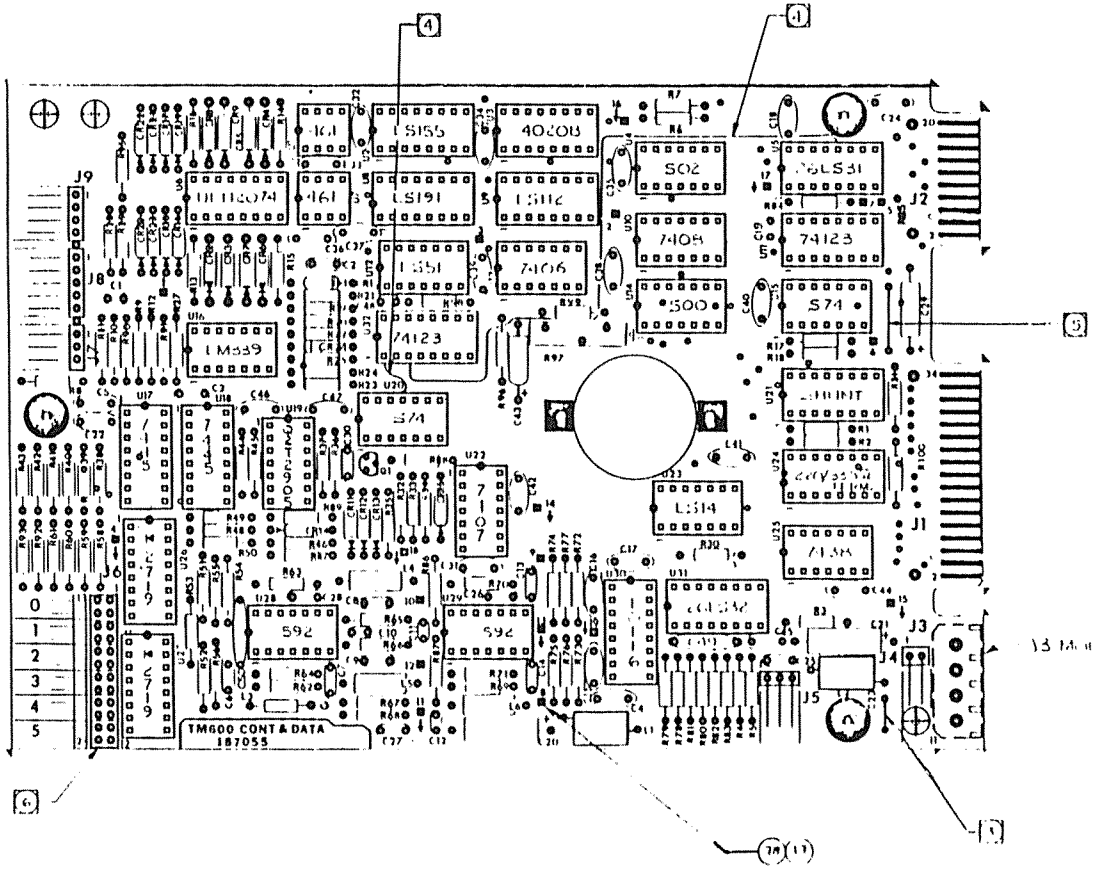
NOTES: UNLESS OTHERWISE SPECIFIED

Tandon CORPORATION

TITLE: CIRCUIT SCHEMATIC TM600 MAIN-μP

SIZE D | DWG NO 187340-001 | REV D


REVISIONS
REV
DESCRIPTION
DATE
DR
CHK
APPR
SEE SHEET 1
-WR GATE
-LCUR
SRDY (IDG)
SC (IC5)
VDET (IB5)
WTW8
+WR DATA
-WR DATA
-HD SEL2
-HD SEL1
-HD SEL0
HD CT0
HD CT1
HD CT2
HD CT3
HD CT4
HD CT5
+HD0
-HD0
+HD1
-HD1
+HD2
-HD2
+HD3
-HD3
+HD4
-HD4
+HD5
-HD5
SHIELD
14,16,18,20,22,24
+5VD
+12VA
Q1 2N4124
CR1
CR10
CR12 1N5231B 5.1V
U20 Q2T2905 (3X)
CAR0 (IC4)
CAR1 (IC4)
NWR (3B8)
READ+ (3D8)
READ- (3D8)
15TPR+
14TPR-
NOTES: UNLESS OTHERWISE SPECIFIED
Tandon
CIRCUIT SCHEMATIC
TM600 MAIN - µP
187340-001
187340-001 TM 600
CIRCUIT SCHEMATIC
2 of 3



DESIGNATOR ASSEMBLY SIDE		
LAST USED		
C18	C19	
CR24	CR10	
J9		
L6		L5-05
Q1		
R100	R258	
TP10		
U32		

REV	DESCRIPTION
B	REV PER E.O. 530017
C	REV PER E.O. 530024
D	REV PER E.O. 530031
E	REV PER E.O. 530066
F	REV PER E.O. 530071
G	REV PER E.O. 530075
J	REV PER E.O. 530092
K	REV PER E.O. 530100
L	REV PER E.O. 530105
M	REV PER E.O. 530107
N	REV PER E.O. 530112
P	REV PER E.O. 530116
R	REV PER E.O. 530120
S	REV PER E.O. 530124
T	REV PER E.O. 530128

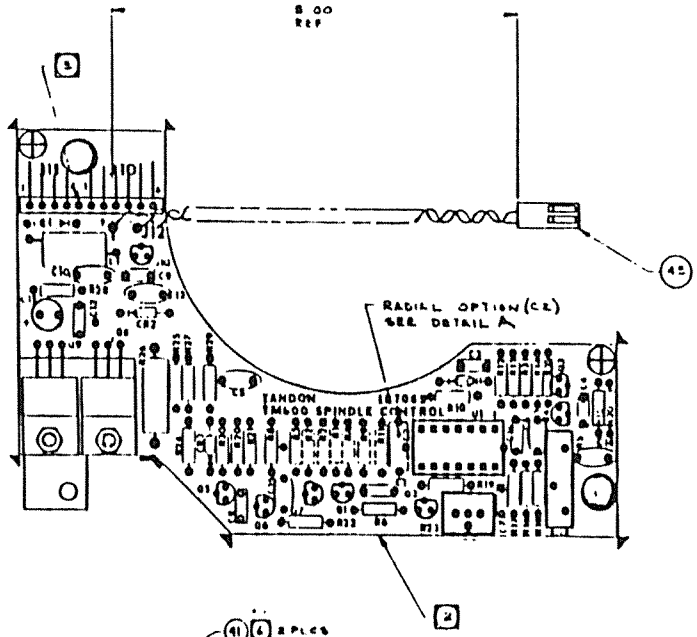
13 MOUNTS ON FARSIDE

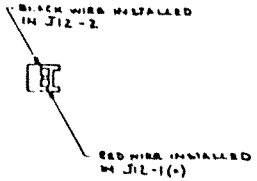
6. RAISE CONNECTOR J6 TO .060 INCHES ABOVE SURFACE PER E.O. 530518.
5. JUMPER PER E.O. 530106.
4. JUMPER PER E.O. 530024.
3. SOLDER #24 AWG INSULATED TIN COATED COPPER WIRE. MAY SUBSTITUTE #24 AWG TEFLON COATED WIRE.
2. REF DOCUMENTS: 187040-001 - CIRCUIT SCHEMATIC
   187042-001 - ARTWORK
1. SEE SHEET 2 FOR PARTS LIST

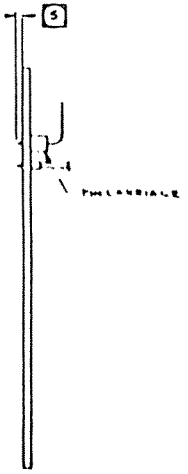
Tandon

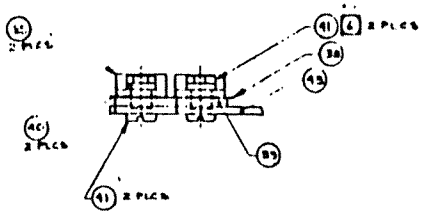
ASSEMBLY, TM600 CONT & DATA

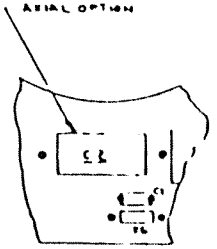
187055-001











DETAIL A

7. REF DOCUMENT : 1B7040-001 CIRCUIT SCHEMATIC
1B7042-001 - ARTWORK

6. TORQUE 4.5 INCH LBS NOMINAL

5. MAX LENGTH OF COMPONENT LEADS BELOW SOLDER SIDE BOARD AFTER ASSEMBLY & TRIMMING SHALL NOT EXCEED .08 INCH.

4. COMPONENT HEIGHT, EXCEPT C11, SHALL NOT EXCEED .65 INCH ABOVE BOARD. CAPACITOR C11, NOT TO EXCEED .80 INCH ABOVE BOARD.

3. CUT PIN TANGENT TO PIN CARRIAGE.

2. THIS ASSEMBLY SHALL BE MADE FROM P.C.B. DETAIL 1B7060-001

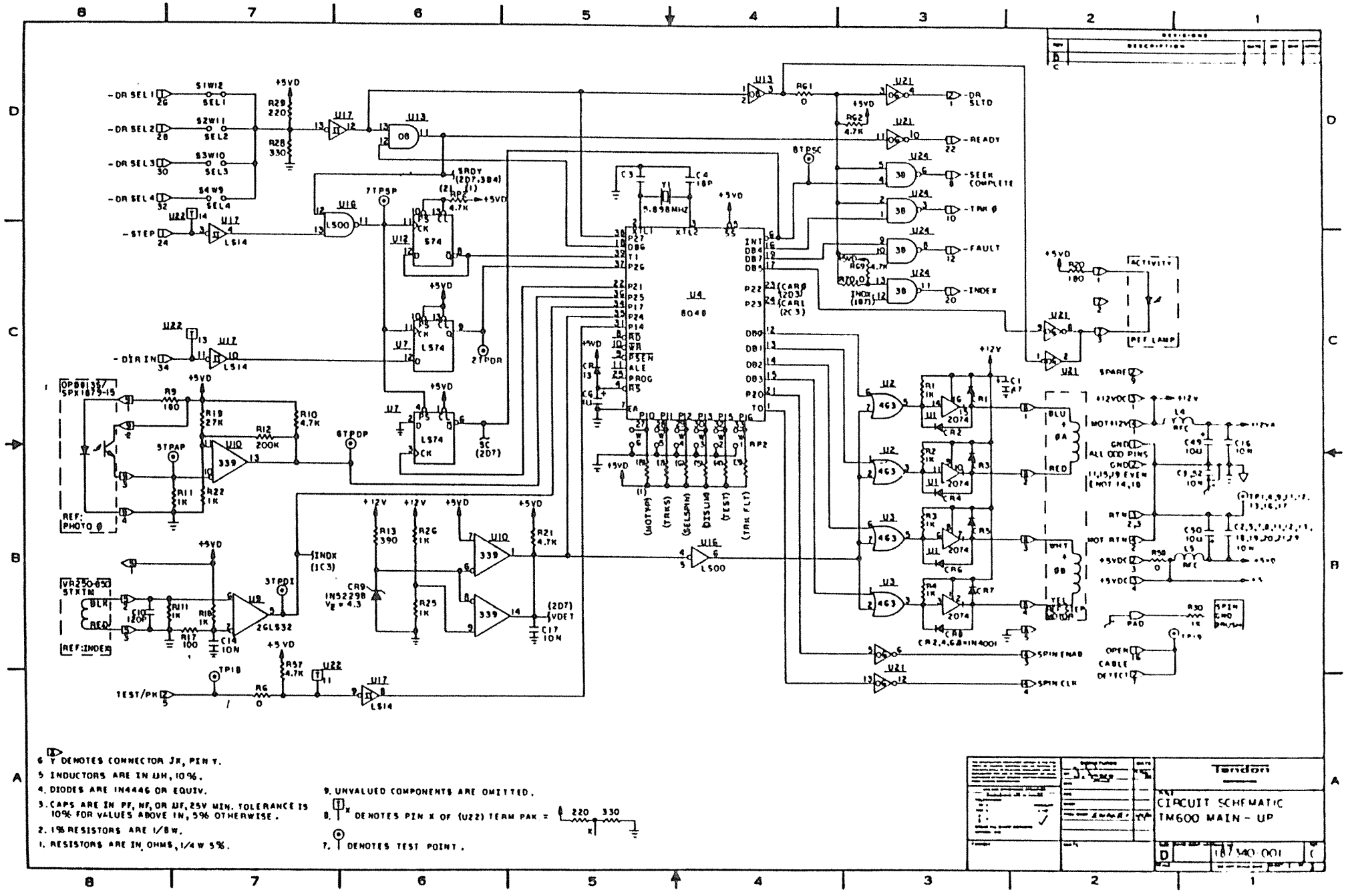
1. ASSEMBLY PER STANDARD MANUFACTURING METHODS.

USED ON TM400

Tandon

SPINDLE CONTROL
ASSY
TM400

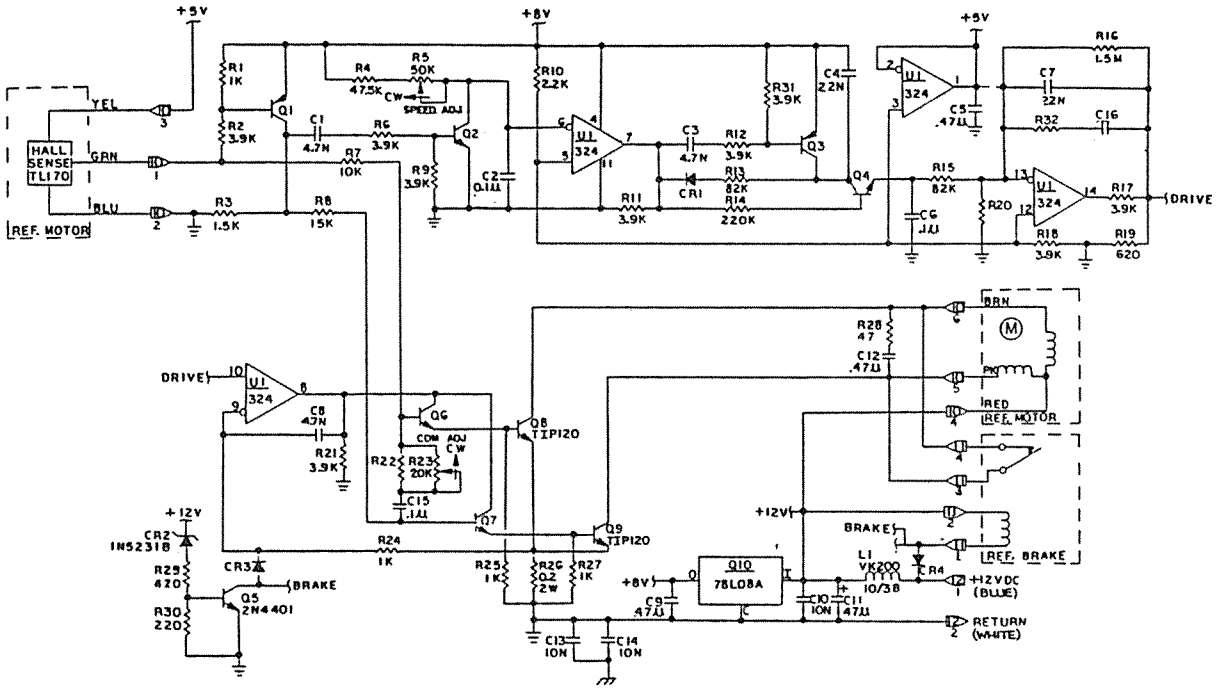
SIZE D



6. Y DENOTES CONNECTOR JX, PIN Y.
5. INDUCTORS ARE IN UH, 10%.
4. DIODES ARE IN4446 OR EQUIV.
3. CAPS ARE IN PF, NF, OR UF, 25V MIN. TOLERANCE IS 10% FOR VALUES ABOVE 1N, 5% OTHERWISE.
2. 1% RESISTORS ARE 1/8W.
1. RESISTORS ARE IN OHMS, 1/4W 5%.

9. UNVALUED COMPONENTS ARE OMITTED.
8. X DENOTES PIN X OF (U22) TERM PAK = 220 330 X
7. DENOTES TEST POINT.

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APP'D
B	REV PER E.O. 11539				
C	REV PER E.O. 11558				
D	REV PER E.O. 530006				
E	REV PER E.O. 530043				
F	REV PER E.O. 530610				
G	REV PER E.O. 530685				



REFERENCE DESIGNATORS	
LAST USED	NOT USED
C16	
CR4	
J3	
L1	
Q10	
R32	
U1	

7. UNVALUED COMPONENTS ARE OMITTED.
6. Y OR Y DENOTES CONNECTOR X, PIN Y.
5. PNP TRANSISTORS ARE 2N4125.
4. NPN TRANSISTORS ARE 2N4124.
3. DIODES ARE IN4446 OR EQUIV.
2. CAPACITORS ARE 25V, 10%, PF, NF, OR UF.
1. RESISTORS ARE IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

SIGNATURES	DATE
DR	
CHK	
ENG	
PROJ. ENGR.	
MATL	

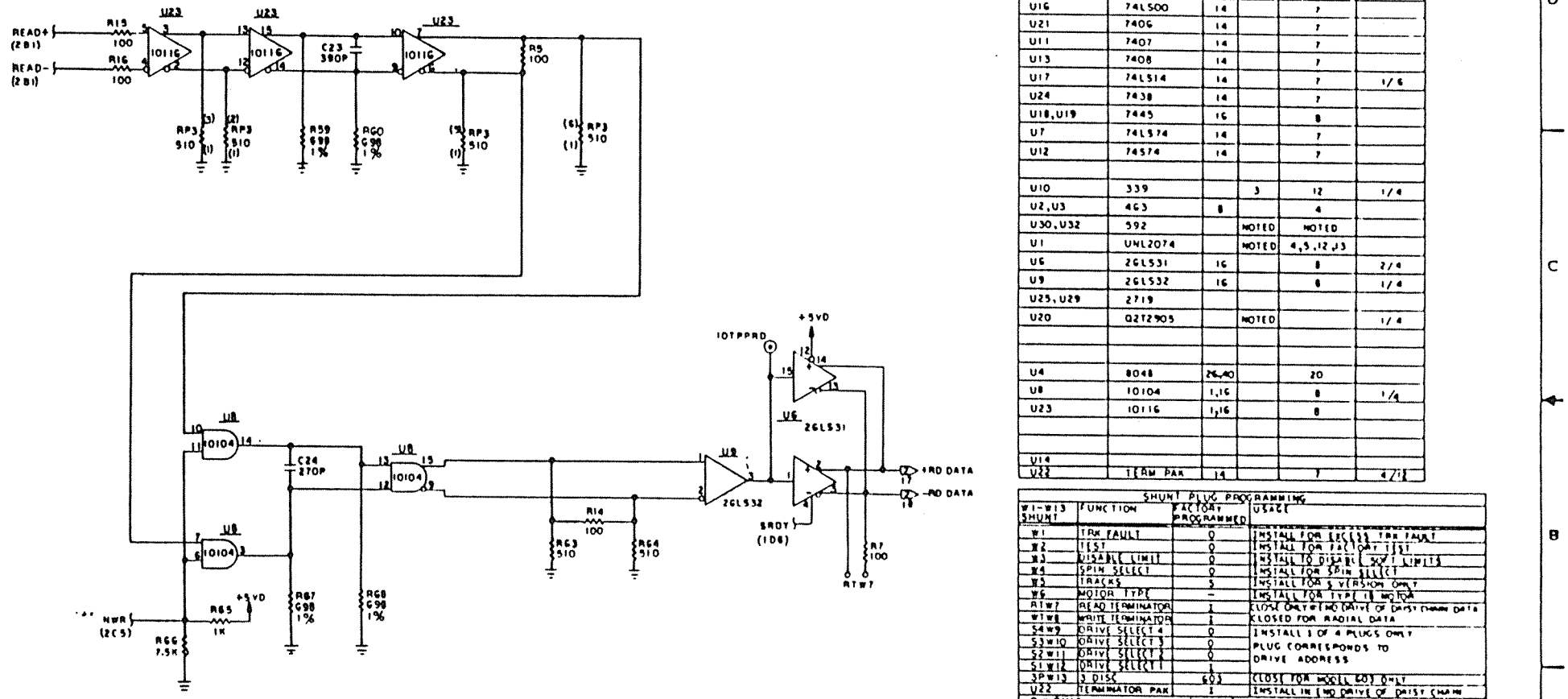
NEXT ASSY | FINIT USE
APPLICATION

Tandon CORPORATION

TITLE
CIRCUIT SCHEMATIC, TM600 SPINDLE CONTROL

SIZE D | DWG. NO. 187060-001 | REV G

SCALE | SHEET 1 OF 1



I.C. LOCATION AND VOLTAGE CHART					
LOCATION	TYPE	#5	#12	GND	UNUSED
U1G	74LS00	14		7	
U21	7406	14		7	
U11	7407	14		7	
U13	7408	14		7	
U17	74LS14	14		7	1/6
U24	7438	14		7	
U18,U19	7445	16		8	
U7	74LS74	14		7	
U12	74S74	14		7	
U10	339		3	12	1/4
U2,U3	4G3	8		4	
U30,U32	592		NOTED	NOTED	
U1	UNL2074		NOTED	4,5,12,13	
U6	26LS31	16		8	2/4
U9	26LS32	16		8	1/4
U25,U29	2719				
U20	Q2T2905		NOTED		1/4
U4	8048	26,40		20	
U8	10104	1,16		8	1/4
U23	10116	1,16		8	
U14					
U22	TERM PAK	14		7	4/7

SHUNT PLUG PROGRAMMING			
W1-W13 SHUNT	FUNCTION	FACTORY PROGRAMMED	USAGE
W1	TRK FAULT	0	INSTALL FOR EXCESS TRK FAULT
W2	TEST	0	INSTALL FOR FACTORY TEST
W3	DISABLE LIMIT	0	INSTALL TO DISABLE SOFT LIMITS
W4	SPIN SELECT	0	INSTALL FOR SPIN SELECT
W5	TRACKS	5	INSTALL FOR 5 VERSION ONLY
W6	MOTOR TYPE	-	INSTALL FOR TYPE 16 MOTOR
RTW7	READ TERMINATOR	1	CLOSE ONLY @ END DRIVE OF DAISY CHAIN DATA
WTW8	WRITE TERMINATOR	1	CLOSED FOR RADIAL DATA
S4W9	DRIVE SELECT 4	0	INSTALL 1 OF 4 PLUGS ONLY
S3W10	DRIVE SELECT 3	0	PLUG CORRESPONDS TO
S2W11	DRIVE SELECT 2	0	DRIVE ADDRESS
S1W12	DRIVE SELECT 1	1	
SPW13	3 DISC	603	CLOSE FOR MODEL 603 ONLY
U22	TERMINATOR PAK	1	INSTALL IN END DRIVE OF DAISY CHAIN

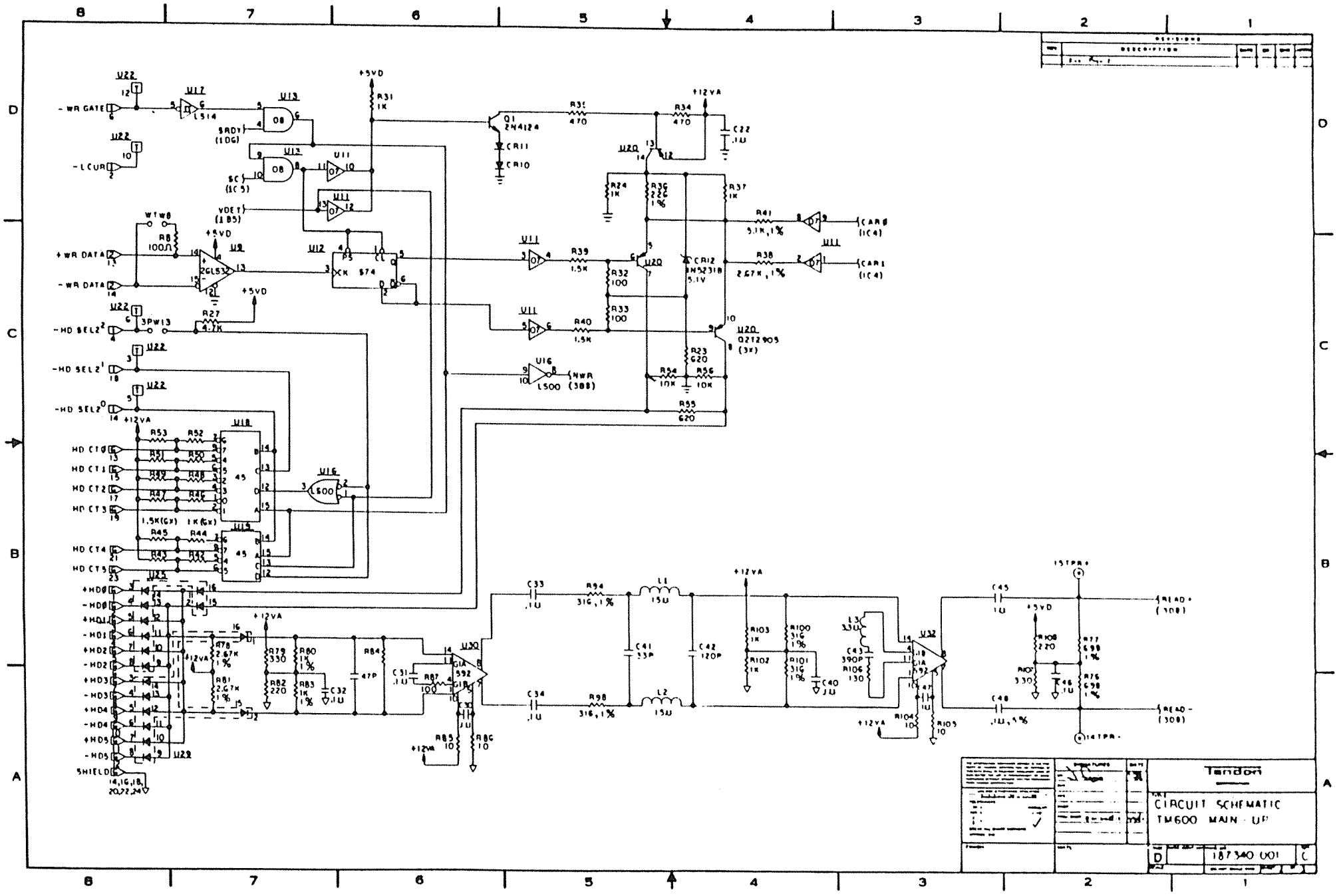
0 = OMIT
1 = INSTALL
5 = CLOSE FOR 5 VERSION ONLY
603 = CLOSE FOR TM603 ONLY

REFERENCE DESIGNATORS	
LAST USED	UNUSED
C53	C15,25-28,35-38,44,51
CR13	
J9	
L5	
Q1	
R111	R71 THRU 75,88-93,95-97,99,109,110
RP3	RP1
TP19	
U32	U5,14,15,20-26,31
W13	
Y1	

Tandon

TITLE
CIRCUIT SCHEMATIC
TM600 MAIN-LIF

D 187340-001


- WR GATE
- LCUR
SRDY (10G)
SC (1C5)
VDET (1B5)
+WR DATA
-WR DATA
-HD SEL2 2
-HD SEL2 1
-HD SEL2 0
HD CT0
HD CT1
HD CT2
HD CT3
HD CT4
HD CT5
+HD0
-HD0
+HD1
-HD1
+HD2
-HD2
+HD3
-HD3
+HD4
-HD4
+HD5
-HD5
SHIELD
14,16,18, 20,22,24
+5VD
+12VA
NWR (3B8)
CAR0 (1C4)
CAR1 (1C4)
READ+ (3D8)
READ- (3D8)
15TPR+
14TPR-
Tandon
CIRCUIT SCHEMATIC
TM600 MAIN - UP
187340 001

CONTENTS

ILLUSTRATIONS

FIGURES

TABLES

ACTIVITY INDICATOR

The activity indicator is located on the front panel of the drive. It is automatically illuminated when the drive is selected.

AIR FILTRATION

A self-contained, recirculating air filtration system supplies clean air through a 0.3-micron filter. A secondary absolute filter is provided to allow pressure equalization with the ambient atmosphere without contamination. The entire head-disk-actuator compartment is maintained at a slightly positive pressure to further ensure an ultraclean environment.

1.4 FUNCTIONAL DESCRIPTION

The drive is fully self-contained and requires no operator intervention during normal operation. During the power-up sequence, the spindle motor reaches 3600 RPM, and the positioning mechanism recalibrates the recording heads back to Track 0. At this time, a Ready signal on the interface indicates the drive is ready for operation.

The head is postioned over the desired track by means of a four-phase stepper motor/band assembly and its associated electronics. This positioner uses a one-step rotation to cause a one-track radial movement. Subsequently, the recording heads can be positioned over the desired cylinders, and the data can be read or written from the appropriate track by selecting the desired head.

Typically, the drive uses MFM write and read data recording methods. Data recovery electronics include a low-level read amplifier, differentiator, a zero-crossover detector, and digitizing circuits. No data decoding feature is provided on the drives.

The drive has the following sensor systems:

1. An optical Track 0 switch senses when the Head/Carriage Assembly is positioned at Track 0.
2. An index sensor, which consists of a magnetic pick-up and index hole positioned to provide an analog signal when an index hole is detected.

1.5 PHYSICAL DESCRIPTION

The TM500 drive is shown in Figure 1-1. The drives contain 130 millimeter storage media that rotate at 3600 RPM, using a direct drive, brushless D. C. motor. The recording is accomplished by noncontact standard recording heads that are moved by a precision split band positioning device and stepper motor.

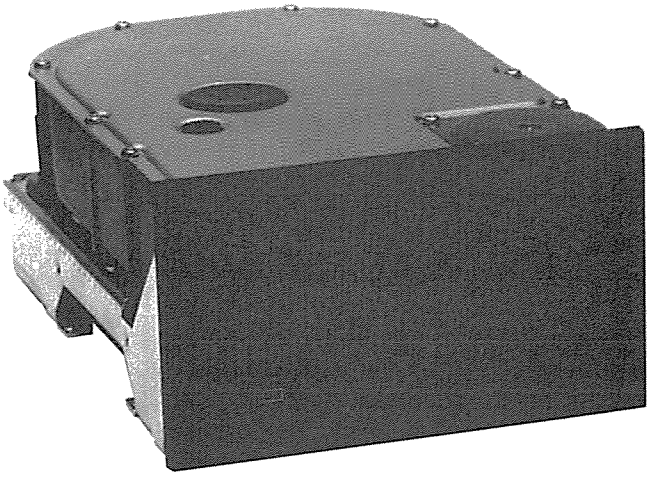


FIGURE 1-1
DISK DRIVE

The Head Disk Assembly is enclosed in a sealed cast aluminum housing, which includes an air filtration system to ensure a contamination-free environment. The housing is shock mounted to a metal frame that has the front panel attached, and threaded holes on the sides and bottom for mounting the drive onto a chassis.

In addition, the drive includes the read/write control electronics, the servo spindle control electronics, an index sensor, a brake assembly, and a front panel indicator.

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This manual provides useful information to assist the customer when incorporating the Tandon rigid disk drive into a system.

Tandon Corporation's TM500 series of drives are full feature, 5-1/4-inch, rigid disk drives. They are compact data storage devices that contain one or more 130-millimeter plated aluminum platters within a sealed housing.

The TM500 series includes Model Numbers TM501, TM502, and TM503, which have one, two, and three recording platters, and use two, four, and six recording heads, respectively.

1.1 SCOPE OF THE DOCUMENT

Section 1 of this manual contains a general description of the disk drives. Section 2 contains the product specifications. Section 3 provides information on operation of the drives.

1.2 PURPOSE OF THE DRIVE

The 5-1/4-inch disk drive is a rotating disk memory device designed for random access data storage and retrieval. Typical applications include word processing systems, entry level microprocessor systems, intelligent calculators, program storage, small business computer systems, and any application in which low cost, random access data storage is required.

1.3 MAJOR FEATURES

MICROPROCESSOR CONTROL

The TM500 series of drives feature an onboard microprocessor. The microprocessor provides five major functions:

1. Self-calibration on power-up.
2. Buffered seek timing for improved access times.
3. Improved positioning with reduced hysteresis.
4. Write current switching for optimal recording quality.
5. Power and track fault detection.

DAISY CHAIN CAPABILITY

The drive provides the address selection and gating functions necessary to daisy chain a maximum of four units at the user's option. The last drive on the daisy chain terminates the interface. The terminations are accomplished by a resistor array plugged into a DIP socket.

INDUSTRY STANDARD INTERFACE COMPATIBILITY

The drive is compatible with controllers that use an industry standard interface.

SECTION 2

PRODUCT SPECIFICATIONS

INTRODUCTION

This section contains the mechanical, electrical and operational, reliability, and environmental specifications for the TM501, TM502, and TM503 disk drives.

2.1 MECHANICAL SPECIFICATIONS

The mechanical and physical dimensions are contained in Figure 2-1.

2.2 ELECTRICAL AND OPERATIONAL SPECIFICATIONS

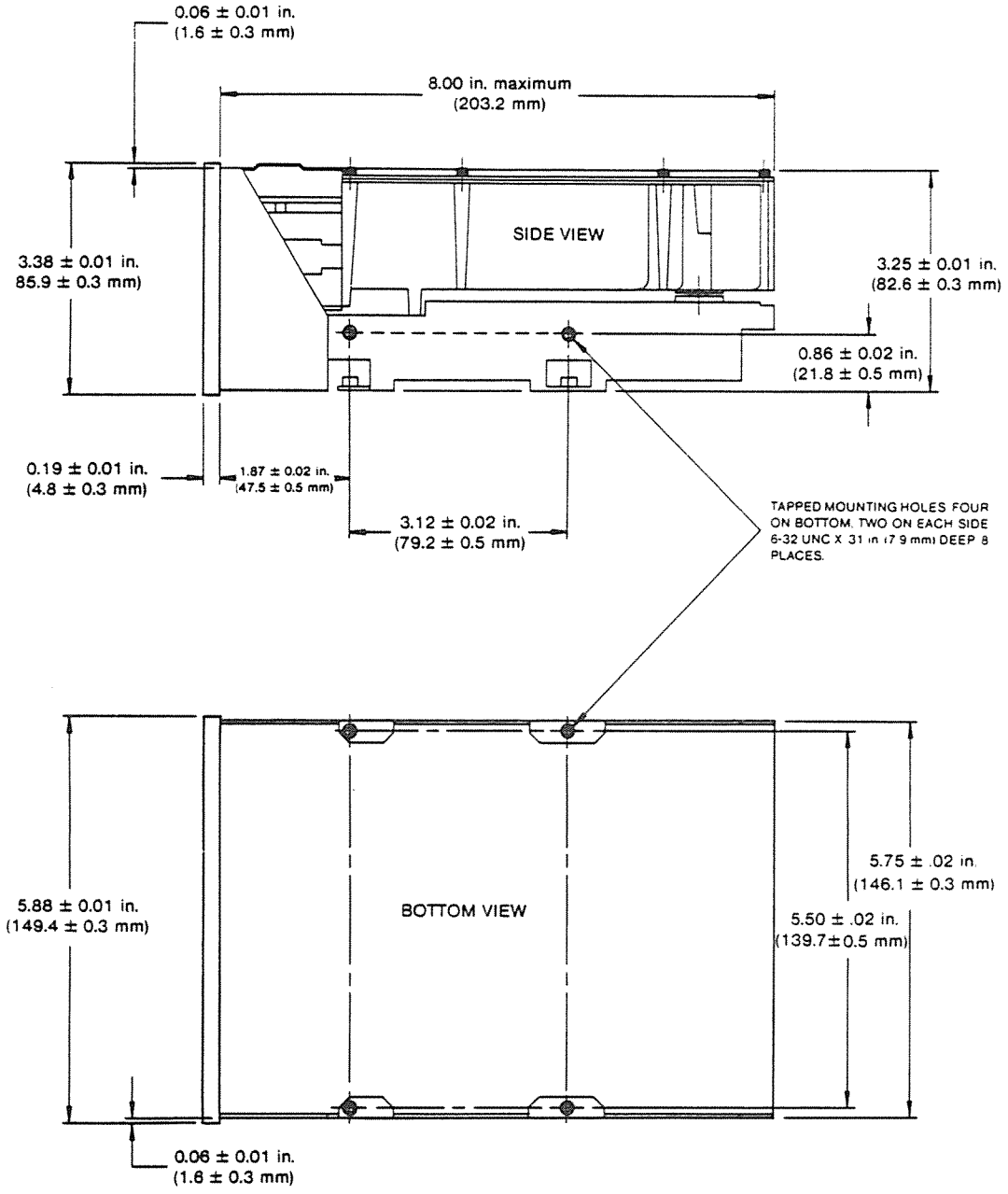
The electrical and operational specifications are contained in Table 2-1. Typical starting current requirements at nominal voltage are contained in Figure 2-2.

2.3 RELIABILITY SPECIFICATIONS

The reliability specifications are contained in Table 2-2.

2.4 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are contained in Table 2-3.



Note: Weight is 3.0 kilograms, 6.5 pounds maximum

FIGURE 2-1
DISK DRIVE OUTLINE DRAWING

TABLE 2-1
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Media	Lubricated, 130 millimeter, plated aluminum disk
Tracks Per Inch	345 TPI
Spacing, Track to Track	2.9 milinches
Number of Cylinders	306 cylinders
Number of Tracks	
TM501	612 tracks
TM502	1224 tracks
TM503	1836 tracks
Disk Speed	3600 RPM ± 1 percent
Average Latency	8.33 milliseconds
Start Time	15 seconds maximum
Stop Time	15 seconds maximum
Seek Time	3 milliseconds track to track
Head Settling Time	15 milliseconds, last track accessed
Average Access Time, Including Head Settling Time, 3 Millisecond Step Rate	321 milliseconds
Average Access Time Using Buffered Seek, Including Head Settling Time	85 milliseconds
Transfer Rate	5 megabits per second

TABLE 2-1 (CONTINUED)
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Maximum Flux Reversal Density	9090 FRPI
Unformatted Capacity Per Drive	
TM501	6.38 megabytes
TM502	12.76 megabytes
TM503	19.14 megabytes
Unformatted Capacity Per Surface	3.19 megabytes
Unformatted Capacity Per Track	10.4 kilobytes

POWER REQUIREMENTS

+12 volts D. C. ±10 percent, 1.5 amperes typical, 5 amperes maximum during motor start-up, not to exceed 12 seconds, 2 amperes maximum running, with no more than 50 millivolts Periodic and Random Deviation (PARD).

+5 volts D. C. ±5 percent, 0.8 amperes typical, 1.2 amperes maximum running, with no more than 50 millivolts PARD.

There are no restrictions in sequencing power supplies on or off.

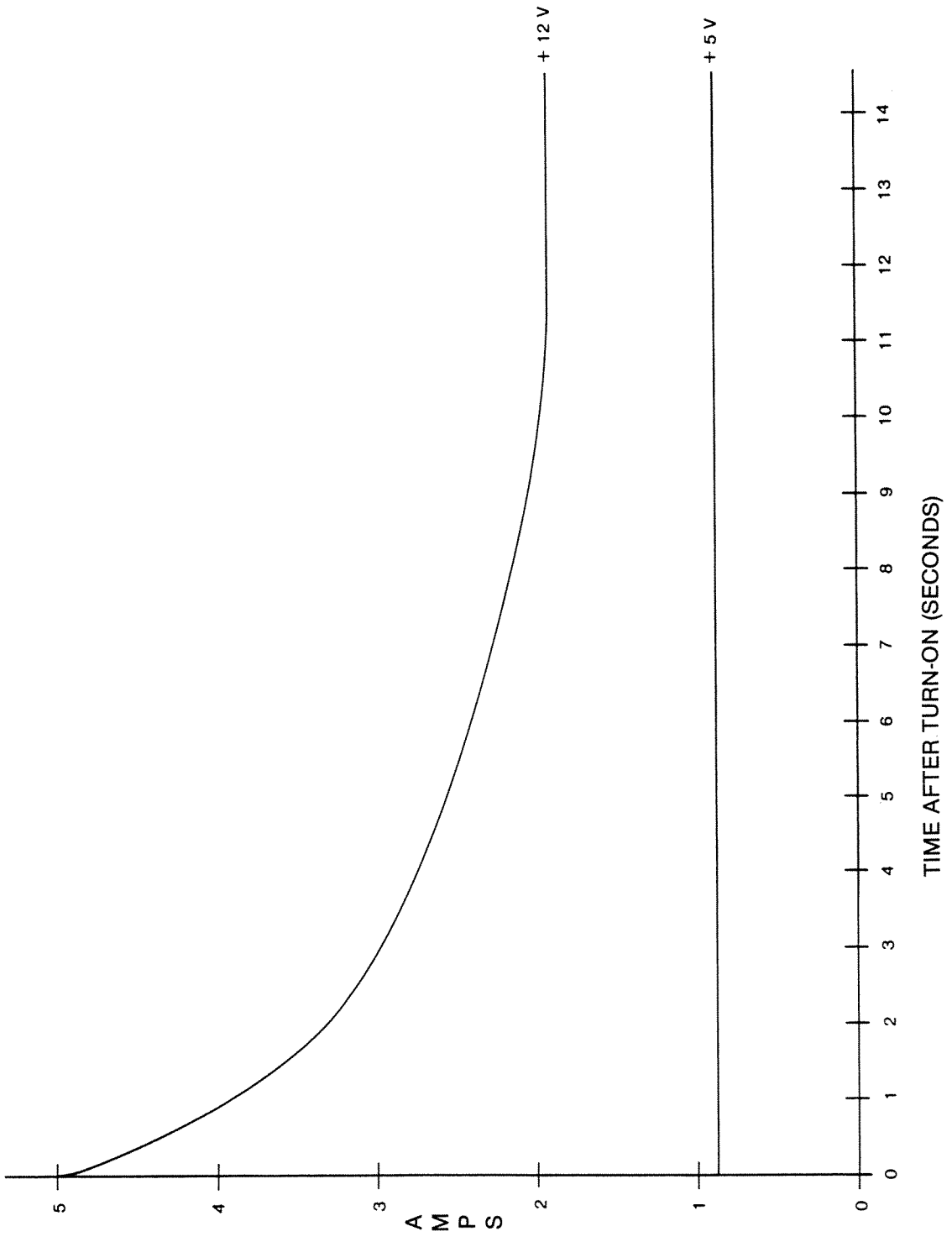


FIGURE 2-2
TYPICAL STARTING CURRENTS

TABLE 2-2
RELIABILTY SPECIFICATIONS

SOFT AND HARD READ ERROR RATES, EXCLUSIVE OF MEDIA DEFECTS

For data that has been verified previously as error free, and when used in conjunction with a data separator and phase lock loop of good design, the recoverable (soft) read error rate for any subsequent read operation shall not exceed one error in 1×10^{10} bits transferred. A recoverable read error is an error that may be corrected within five attempts to reread the data.

The nonrecoverable (hard) read error rates shall not exceed one error in 1×10^{12} bits transferred. A nonrecoverable read error is an error that may not be corrected within five attempts to reread data, providing that the writing of the data previously has been verified as correct. The seek error rate is not to exceed one error in 1×10^{6} seeks.

MEDIA DEFECTS

Any defects on the media surface will be identified on a defect map provided with each drive. This defect map will indicate the head number, track number, and number of bytes from index for each defect. Each defect shall be no longer than 16 bits. Cylinders 000 and 001 are guaranteed error free.

The map is offered as a guide only. The number of defects and their location can change due to customer system variations such as data separators.

Mean Time Between Failures	11,000 power on hours
Mean Time To Repair	30 minutes
Component Design Life	5 years
Preventative Maintenance	Not required

TABLE 2-3
ENVIRONMENTAL SPECIFICATIONS

Ambient Temperature	
Operating	4°C to 50°C, 39°F to 122°F
Nonoperating	-40°C to 60°C, -40°F to 140°F
Temperature Gradient	
Operating	10°C per hour, 18°F per hour
Nonoperating	Below that causing condensation
Relative Humidity	8-to-80 percent, noncondensing
Relative Humidity Gradient	
Operating	20 percent per hour
Nonoperating	Below that causing condensation
Maximum Wet Bulb Temperature	26°C, 78.8°F, without condensation
Elevation	
Operating	Density Altitude: -457 to 2,972 meters, -1,500 to 9,750 feet
Nonoperating	Sea level to 3,650 meters, Sea level to 12,000 feet

SECTION 3

OPERATION

INTRODUCTION

This section contains information pertinent to the handling, inspection, installation, and operation of the TM500 series of drives.

3.1 UNPACKING THE DRIVE

Each drive is shipped in a protective container which, when bulk packaged, minimizes the possibility of damage during shipment.

Visually examine the shipping container for possible damage. Notify the carrier immediately if any damage is found.

The following procedure is recommended for unpacking the drive.

1. Place the shipping container on a flat work surface.
2. Cut the tape on the shipping container.
3. Remove the foam lid and pads from the shipping container.
4. Remove the inner container.
5. Remove the drive from the inner container.
6. Place the drive on a foam lined surface.

CAUTION
Do not manually rotate the stepper motor or spindle motor. Damage to the heads and disk may result.

NOTE
The inside chamber of the drive is a sealed compartment that must not be opened.

When returning the drive to the service center, be sure to use prior steps in reverse order, and ensure the foam stiffeners are in the proper location, with the cardboard dividers properly in place between the drives (see Figure 3-1).

3.2 PREINSTALLATION CHECKOUT

Before applying power to the drive, inspect for the following:

1. Ensure the front panel is secure.
2. Ensure the circuit board is secure.
3. Ensure the connectors are firmly seated.
4. Ensure there is no debris or foreign material between the frame and the head/disk casting.
5. Ensure the head/disk housing can move freely on the shock mounts of the frame.
6. Ensure the termination resistor pack and jumper blocks are firmly seated and in the correct configuration.

3.3 MOUNTING THE DRIVE

The drive can be mounted in any vertical or horizontal plane. Eight 6-32 tapped holes are provided for mounting: two on each side and four on the bottom of the frame (see Figure 2-1, page 2-2). The drive is manufactured with some critical internal alignments that must be maintained. Hence, it is important the mounting hardware does not introduce significant stress on the drive.

Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted. Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances.

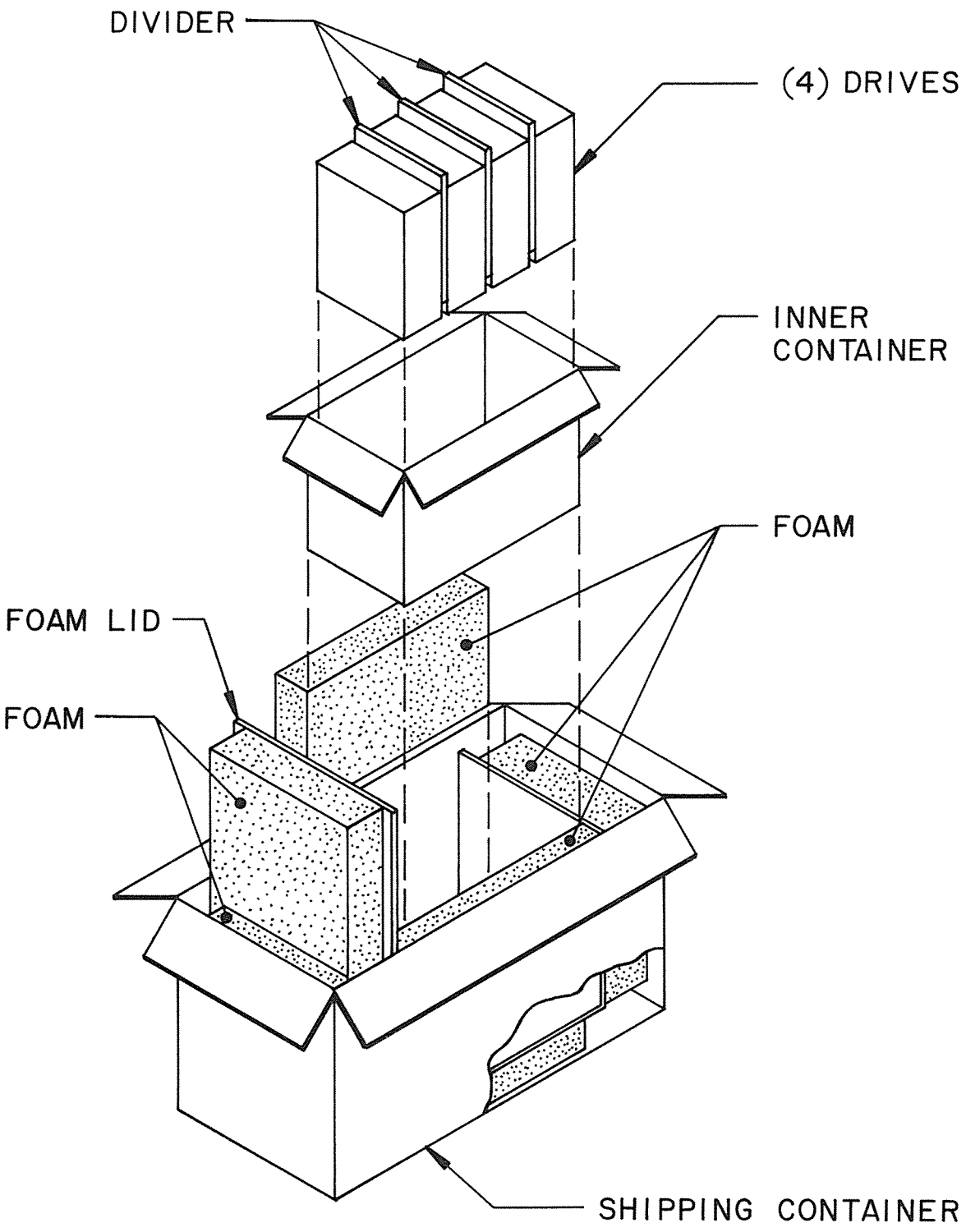


FIGURE 3-1
FOUR PACK SHIPPING CONTAINER

DUST COVER

The design of an enclosure should incorporate a means to prevent contamination from loose items, e.g., dust, lint, and paper chad since the drive does not have a dust cover.

FREE AIR FLOW

When the drive is mounted so the components have access to the free flow of air, normal convection cooling allows operation over the specified temperature range (see Table 2-3, page 2-7).

CONFINED ENVIRONMENT

When the drive is mounted in a confined environment, air flow must be provided to maintain specified air temperatures in the vicinity of the motors and the circuit boards.

3.4 INTERFACE CONNECTORS

The electrical interface between the drive and the host system is via three connectors. J1 provides control signals for the drive (see Figure 3-2). J2 provides for the radial connection of read/write data signals (see Figure 3-3). J3 provides for D.C. power (see Figure 3-4).

Table 3-1 contains interface lines. The interface description of the connectors, and the location of each, is contained in this section.

J1/P1 CONNECTOR

Connection to J1 is through a thirty-four-pin circuit board connector. Figure 3-2 contains the dimensions of this connector. The pins are numbered 1 through 34. The even pins are located on the component side of the circuit board. Pin 2 is located on the end of the circuit board connector closest to the D. C. power connector J3/P3, and is labeled. A key slot is provided between Pins 4 and 6. The recommended mating connector for P1 is 3M ribbon connector P/N 3463-0001, without ears.

J2/P2 CONNECTOR

Connection to J2 is through a 20-pin circuit board edge connector. Figure 3-3 contains the dimensions of this connector. The pins are numbered 1 through 20. The even pins are located on the component side of the circuit board. The recommended mating connector for P2 is 3M ribbon connector P/N 3461-0001, without ears. A key slot is provided between Pins 4 and 6.

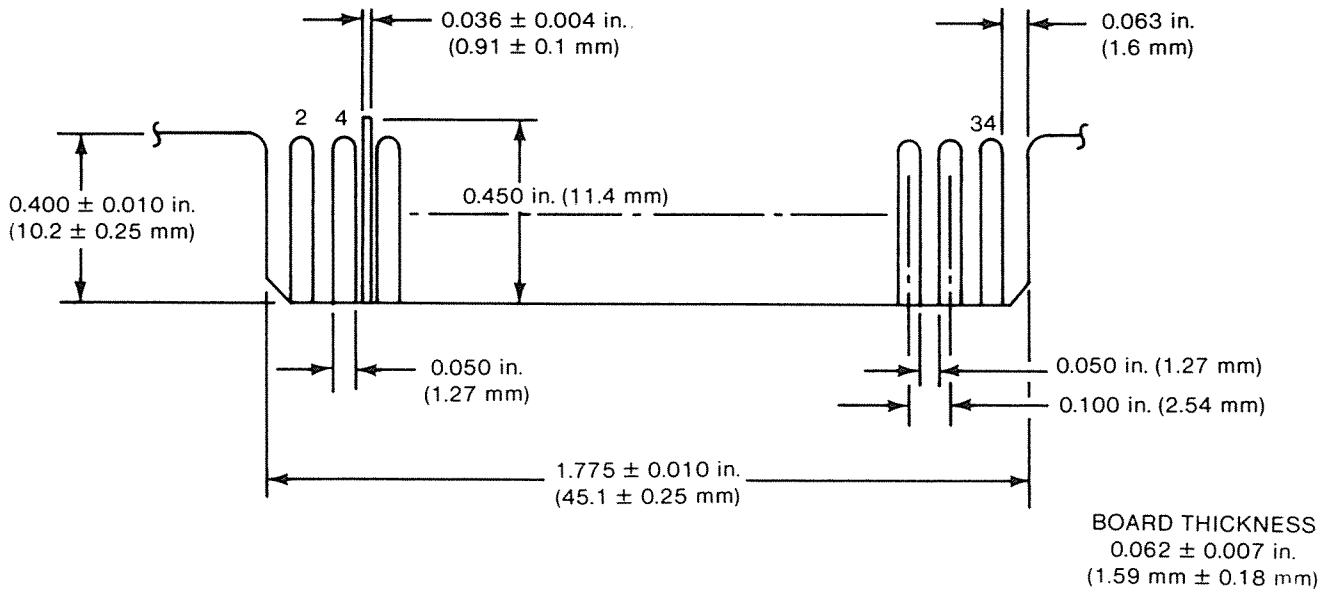


FIGURE 3-2
J1 EDGE CONNECTOR DIMENSIONS

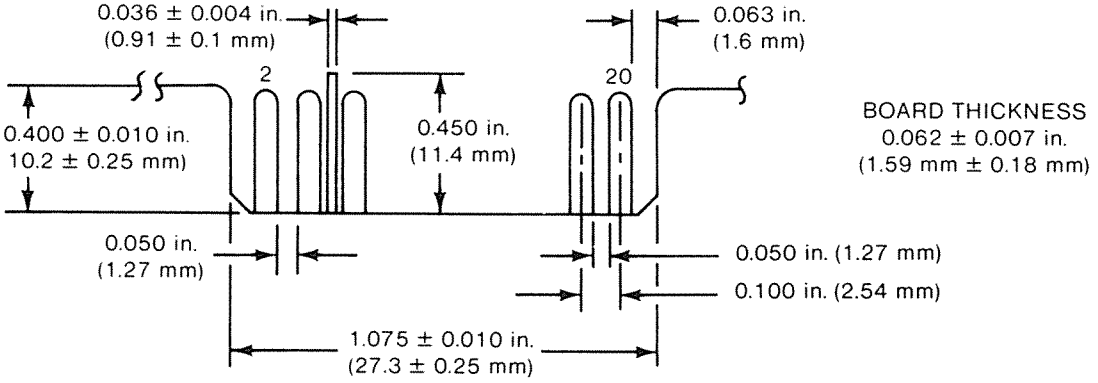


FIGURE 3-3
J2 EDGE CONNECTOR DIMENSIONS

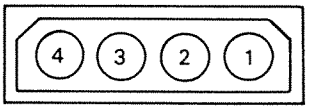


FIGURE 3-4
J3 POWER CONNECTOR

TABLE 3-1
DRIVE INTERFACE SIGNALS AND PIN ASSIGNMENTS

Connector	Interface Pin Number: Signal	Ground	Signal Type	I/O	Name of Signal
P1	2	(1)	S	I	Spare
↑	4	(3)	S	I	Head Select 2^2
	6	(5)	S	I	Write Gate
	8	(7)	S	O	Seek Complete
	10	(9)	S	O	Track 0
34-Pin	12	(11)	S	O	Fault
Ribbon	14	(13)	S	I	Head Select 2^0
Daisy	16	(15)	—	—	Reserved (To J2 - 7)
Chain	18	(17)	S	I	Head Select 2^1
↓	20	(19)	S	O	Index
	22	(21)	S	O	Ready
	24	(23)	S	I	Step
	26	(25)	S	I	Drive Select 0
	28	(27)	S	I	Drive Select 1
	30	(29)	S	I	Drive Select 2
	32	(31)	S	I	Drive Select 3
P1	34	(33)	S	I	Direction In
P2	1	(2)	S	O	Drive Select
↑	3	(4)	S	—	Spare
	5	(6)	—	—	Reserved
	7	(8)	—	—	Reserved (To J1-16)
20-Pin	9	(10)	—	—	Spare
Ribbon	11	(12)	—	—	Ground
Radial	13	—	D	I	+ Write Data
↓	14	—	D	I	− Write Data
	15	(16)	—	—	Ground
	17	—	D	O	+ Read Data
	18	—	D	O	− Read Data
P2	19	(20)	—	—	Ground
P3	1			—	+ 12 volts D. C. In
↑	2			—	+ 12 volts D. C. Return
Radial	3			—	+ 5 volts D. C. Return
P3	4			—	+ 5 volts D. C. In

NOTES:
1. S — Single Ended
2. D — Differential
3. I — Drive Input
4. O — Drive Output

J3/P3 CONNECTOR

D. C. power connector J3 is a four-pin AMP Mate-N-Lok connector, P/N 350211-1, mounted on the solder side of the circuit board. The recommended mating connector, P3, is AMP P/N 1-480424-0, utilizing AMP pins P/N 60619-4. J3 pins are labeled on the J3 connector (see Figure 3-4). J3 cabling must be 18 AWG, minimum.

FRAME GROUND CONNECTOR

The frame ground connector is Faston AMP P/N 61761-2. The recommended mating connector is AMP P/N 62187-1. To realize error rates (see Table 2-2), it must be connected directly to the centrally located system ground via an 18 AWG, minimum, cable.

3.5 INTERFACE LINE DESCRIPTIONS

The interface for the TM500 series drive is available in one configuration. It is compatible with industry standard drives. Compatibility is defined as using the same pin assignment where the signal and function are common. Table 3-1 contains pin assignments.

The interface may be connected in the radial or daisy chain configuration (see Figures 3-5 and 3-6).

INPUT CONTROL SIGNALS

The input control signals are of two kinds: those to be multiplexed in a multiple drive system and those that do the multiplexing. The input control signals to be multiplexed are: Reduced Write Current, Write Gate, Head Select Line 2^0, Head Select Line 2^1, Head Select Line 2^2, Step, and Direction In. The multiplexing signal is Drive Select 0, Drive Select 1, Drive Select 2 or Drive Select 3.

The input signals have the following electrical specifications, as measured at the drive. Figure 3-7 illustrates the recommended circuit.

True: 0.0 volt D. C. to 0.4 volt D. C. at I = -40 milliamperes, maximum

False: 2.5 volts D. C. to 5.25 volts D. C. at I_L = 250 microamperes, maximum (open)

All input signals share a 220/330 ohm resistor pack for line termination. Only the last drive in the chain should have the resistor pack installed.

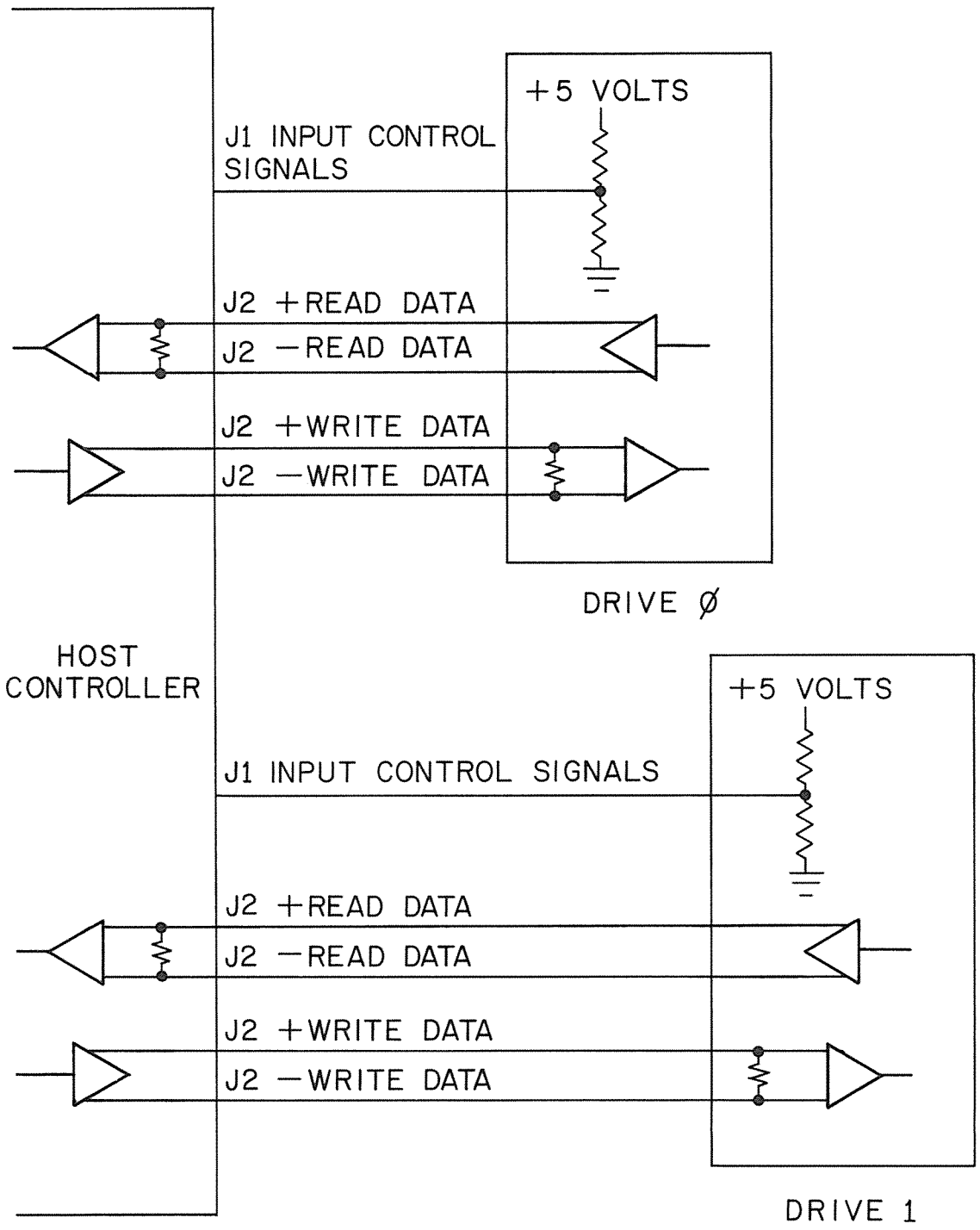


FIGURE 3-5
RADIAL CONFIGURATION

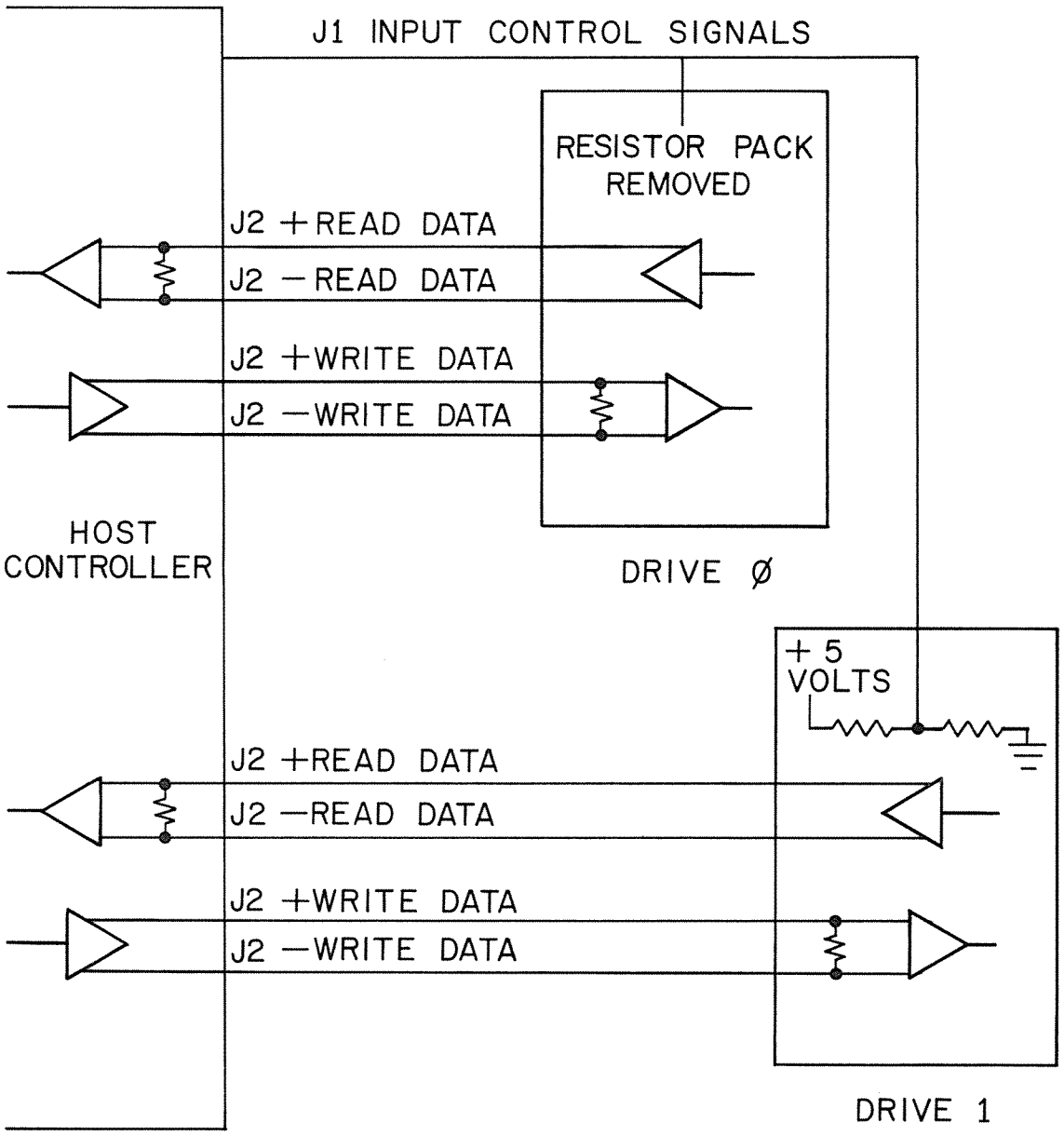


FIGURE 3-6
DAISY CHAIN CONTROL LINES

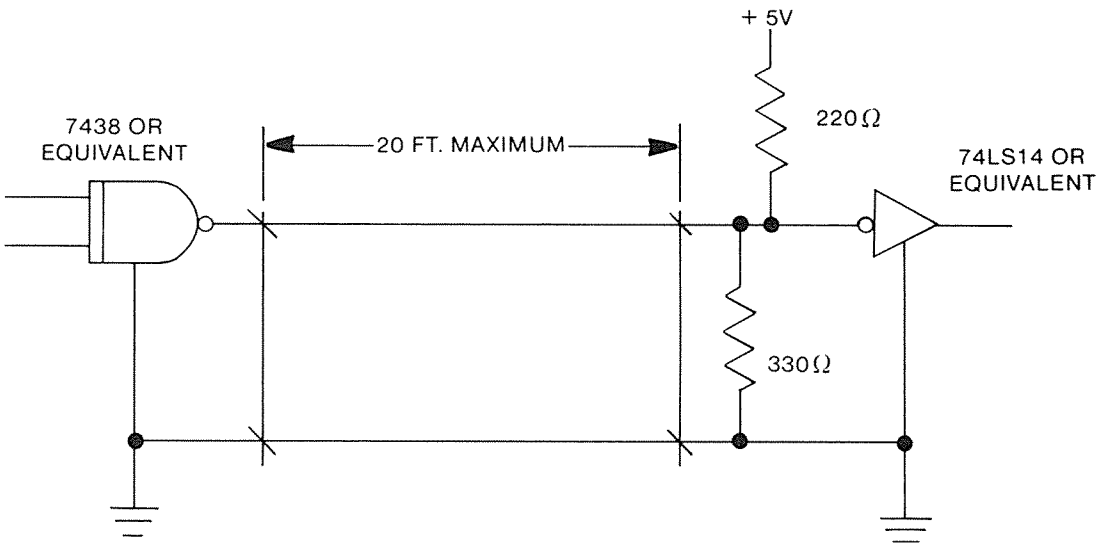


FIGURE 3-7
CONTROL SIGNAL/DRIVER RECEIVER CIRCUIT COMBINATION

WRITE GATE

The active state of this signal or logical zero level enables write data to be written on the disk. The inactive state of this signal enables the data to be transferred from the drive. In addition, the inactive state enables the step pulse to step the read/write actuator.

HEAD SELECT LINES 2^0, 2^1, 2^2

These three lines provide for the selection of each read/write head in a binary coded sequence. Head Select Line 2^0 is the least significant line. The heads are numbered 0 through 5. When all Head Select Lines are false, Head 0 is selected. Table 3-2 describes which head is selected for the head select lines.

TABLE 3-2
HEAD SELECT LINES

Head Select Line			Head Selected	
2^2	2^1	2^0	Jumper 3 PW13 OUT TM501, TM502	Jumper 3 PW13 IN TM503
1	1	1	0	0
1	1	0	1	1
1	0	1	2	2
1	0	0	3	3
0	1	1	0	4
0	1	0	1	5
0	0	1	2	0
0	0	0	3	1

Head recovery time (head-to-head select, write-to-read recovery, or read-to-write recovery) is 2.4 microseconds maximum.

STEP

This interface line is a control signal that causes the read/write heads to move with the direction of motion defined by the Direction In line.

The access motion is initiated at the logical true-to-logical false transition or the trailing edge of this signal pulse. Any change in the Direction In line must be made at least 100 nanoseconds before the true-to-false edge of the step pulse. The quiescent state of this line should be held logically false.

The read/write head moves at the rate of the incoming step pulses. The minimum time between successive steps is three milliseconds, except during execution of a buffered seek. The minimum pulse width is one microsecond. Figure 3-8 illustrates the step timing.

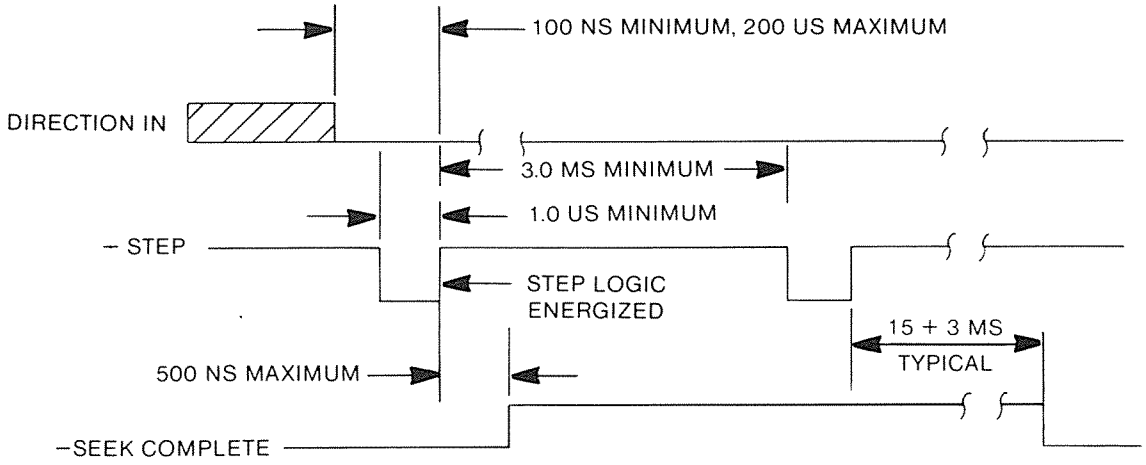


FIGURE 3-8
STEP MODE TIMING

BUFFERED SEEK

The buffered seek uses an onboard microprocessor that calculates the most efficient seek algorithm for the user. The user need only issue step pulses in accordance with the timing shown (see Figure 3-9). Step pulses are issued in a 1:1 ratio to the cylinders moved. If more pulses are issued than there are cylinders left to move, the heads soft stop at the last cylinder.

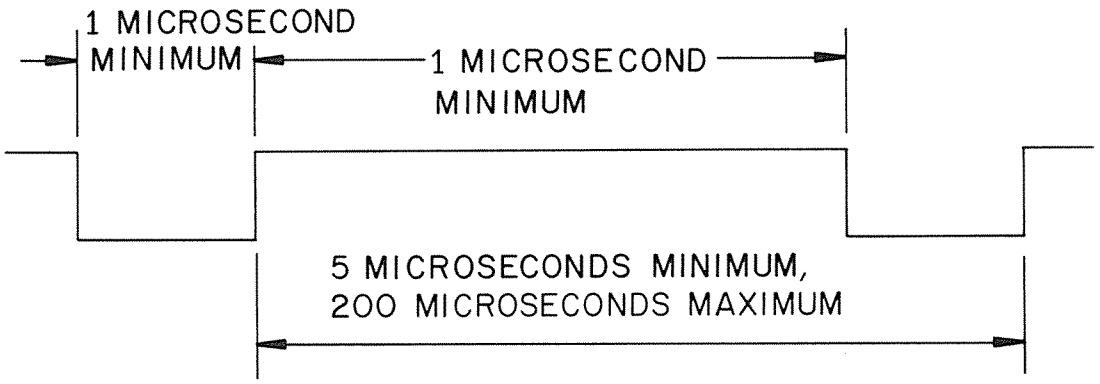


FIGURE 3-9
BUFFERED SEEK STEP PULSES

DIRECTION IN

This signal defines the direction of motion of the read/write head when the Step line is pulsed. An open circuit or logical false defines the direction as "out". If a pulse is applied to the Step line, the read/write heads move away from the center of the disk. If this line is true, the direction is defined as "in", and the read/write heads move in toward the center of the disk.

Seek Complete must be true prior to changing directions and the application of additional step pulses.

REDUCED WRITE CURRENT

The Reduced Write Current input line is terminated, but is not used in the TM500 series drives. The microprocessor automatically switches write current.

DRIVE SELECT 0 THROUGH DRIVE SELECT 3

These control signals enable the selected drive's input receivers and output drivers. When logically false, the output drivers are open circuits and the input receivers do not acknowledge signals presented to them.

Selecting the appropriate jumper block at W9 through W12 determines which select line activates the drive.

NOTE
Only one drive may be selected at a time.

OUTPUT CONTROL SIGNALS

The output control signals are driven with an open collector output stage capable of sinking a maximum of 40 milliamperes in a true state, with a maximum voltage of 0.4 volt measured at the driver. When the line driver is in the false state, the driver transistor is off, and the collector cutoff is a maximum of 250 microamperes.

All J1 output lines are enabled by the respective Drive Select lines.

SEEK COMPLETE

The Seek Complete signal goes true when the read/write heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when Seek Complete is false.

Seek complete goes false:

1. When a recalibration sequence is initiated by the microprocessor at power on because the read/write heads are not over Track 0.
2. 500 nanoseconds, maximum, after the trailing edge of a step pulse or a series of step pulses.
3. When power is momentarily lost, Seek Complete is false when power is restored and remains false until an automatic recalibration is completed.

TRACK 0

The Track 0 signal indicates a true state only when the drive's read/write heads are positioned at Track 0, the outermost data track.

FAULT

The Fault signal is used to indicate a condition exists in the drive that could cause improper writing on the disk. When this line is true, further writing is inhibited, as are other drive functions, until the condition is corrected.

This condition is caused by either the +12 volt or +5 volt supply dropping below the specified limits, and on power up until a successful recalibration sequence is completed.

INDEX

The Index signal is provided once each revolution, 16.7 milliseconds nominal, to indicate the beginning of the track. Normally, this signal is false and makes the transition to true to indicate Index. Only the transition from logical false to logical true is valid.

READY

When true, the Ready signal, together with Seek Complete, indicates that the drive is ready to read, write or seek, and the I/O signals are valid. When this line is false, all controller-initiated functions are inhibited.

The typical time after power on for Ready to be true is fifteen seconds. Track 0, Seek Complete, and Ready come true sequentially during power on.

SELECT STATUS

A Status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The Drive Selected line is driven by a TTL open collector drive (see Figure 3-7). This signal goes active only when the drive is programmed as Drive X, X = 0, 1, 2, or 3, by programming the shunt on the drive, and the Drive Select X line at J1/P1 is activated by the host system.

DATA TRANSFER SIGNALS

All lines associated with the transfer of data between the drive and the host system are differential in nature and may be multiplexed. These lines are provided at the J2/P2 connector on all drives. Signal levels are defined by RS-422A.

Two pairs of balanced lines are used for the transfer of data: MFM Write Data and MFM Read Data. Figure 3-10 illustrates the driver/receiver combination used with the drive for data transfer signals.

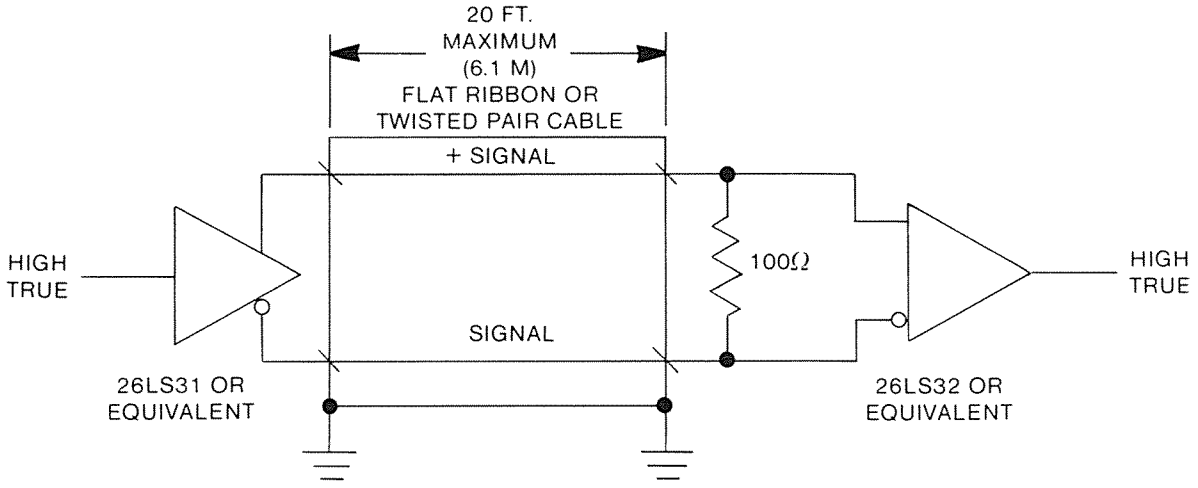


FIGURE 3-10
DATA TRANSFER LINE DRIVER RECEIVER

MFM WRITE DATA

This is a differential pair of lines that define the flux transition to be written on the track. The transition of the +MFM Write Data line going more positive than the —MFM Write Data line causes a flux reversal on the track if Write Gate is active. This signal must be driven to an inactive state, +MFM Write Data more negative than —MFM Write Data, by the host system when in a read mode.

The delay from the leading edge of Write Gate to the Write Data pulse is 400 nanoseconds, maximum.

MFM READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system via the differential pair of MFM Read Data lines. The transition of the +MFM Read Data line going more positive than the -MFM Read Data line represents a flux reversal on the track of the selected head.

3.6 DRIVE ADDRESS AND OPTION SELECTION

The drive address and option selection is determined by the programmable jumper blocks located on the logic circuit board. If jumper configurations are changed, power should be cycled off and on, so that the microprocessor can recognize the new configuration.

The option programming guide is contained in Table 3-3

3.7 SHIPPING PACK AND HANDLING

Figures 3-11 through 3-13 provide basic information on recommended design guidelines for packaging systems.

From various drop tests conducted, it has been established that drives subjected to shock loads in excess of twenty G's may be damaged and consequently not meet published performance specifications for data reliability, margins, and function.

In order to avoid media or head damage, it is recommended that:

1. Drive mounting designs incorporate some type of shock dampening consideration.

2. Shipping cartons protect the drive within the system to withstand twenty G's.

3. Individual drives are handled carefully, e.g., receiving and in-process personnel are properly trained, surface mats are used on working surfaces to prevent the possibility of "handling shock," and padding is placed on racks and carts.

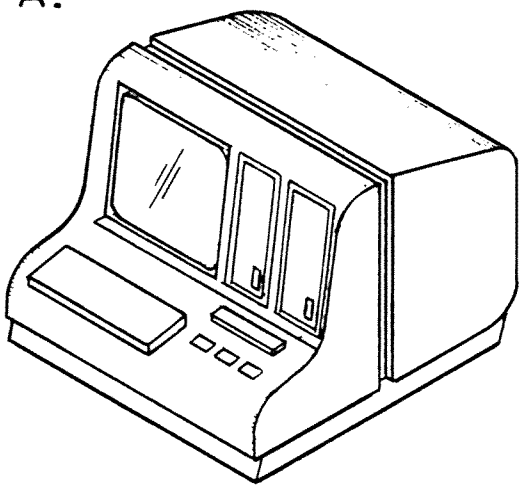
Please emphasize the critical aspects of handling these drives to all concerned people. In addition, Tandon provides technical assistance on packing and handling to customers upon request.

TABLE 3-3
OPTION PROGRAMMING GUIDE

W1 - W3 Jumper	Function	Factory Programmed	Usage
W1	Track Fault	O	Install for excess track fault.
W2	Test	O	Install for factory test.
W3	Disable Limit	O	Install to disable soft limits.
W4	Spin Select	O	Install for spin select.
W5	Tracks	S	Install for standard version only.
W6	Motor Type	—	Install for Type 1.8^0 motor.
RTW7	Read Terminator	I	Close only at end drive of daisy chain data. Closed for radial data.
WTW8	Write Terminator	I	
S4W9	Drive Select 4	O	Install one of four plugs only. Plug corresponds to drive address.
S3W10	Drive Select 3	O	
S2W11	Drive Select 2	O	
S1W12	Drive Select 1	I	
3PW13	Three Disk	503	Close for Model TM503 only.
U22	Terminator Pack	I	Install in end drive of daisy chain.

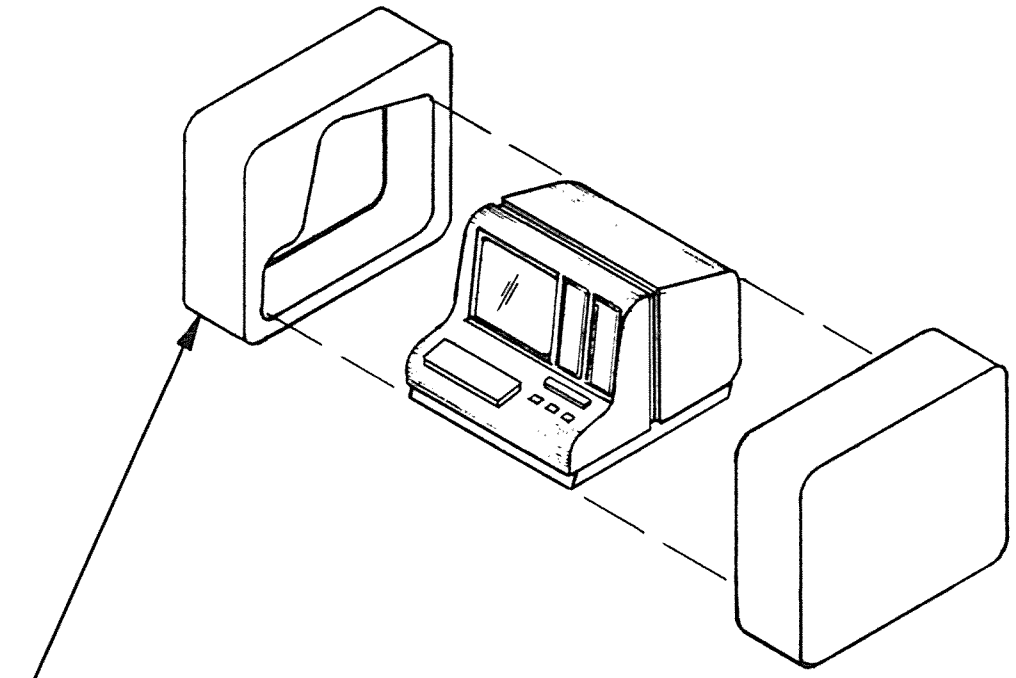
NOTES:
- O = Omit
- I = Install
- S = Close jumper for standard version only.
- 503 = Close jumper for TM503 only.

STEP A.



ENCLOSE UNIT IN POLY BAG TO AVOID SURFACE SCRATCHES AND OTHER DAMAGE

STEP B.



MOLD POLYURETHANE "CLAMSHELL" TO "CUBE" UNIT

FIGURE 3-11
RECOMMENDED SHIPPING PACK DESIGN, CONFIGURATION 1

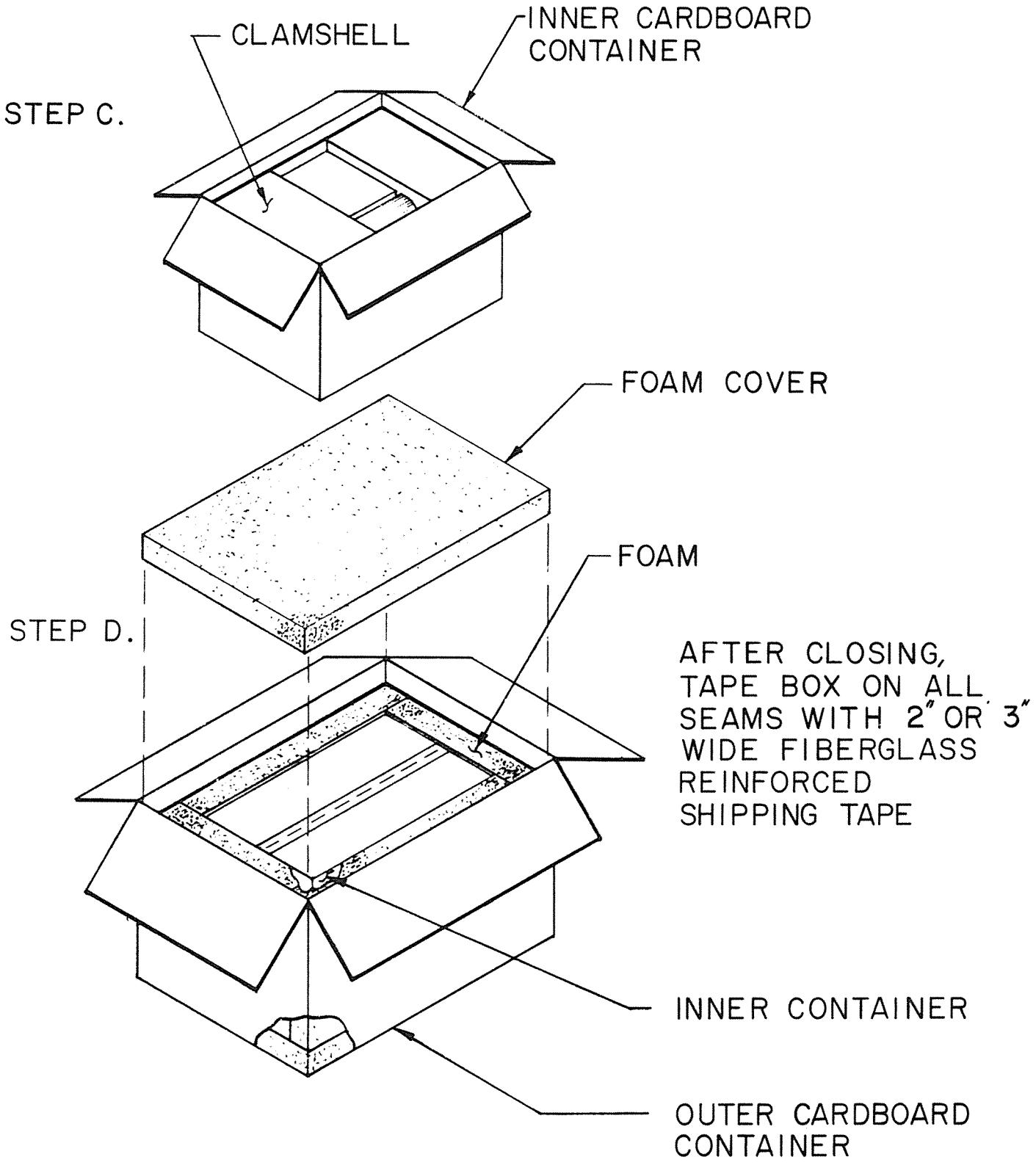


FIGURE 3-11 (CONTINUED)
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 1

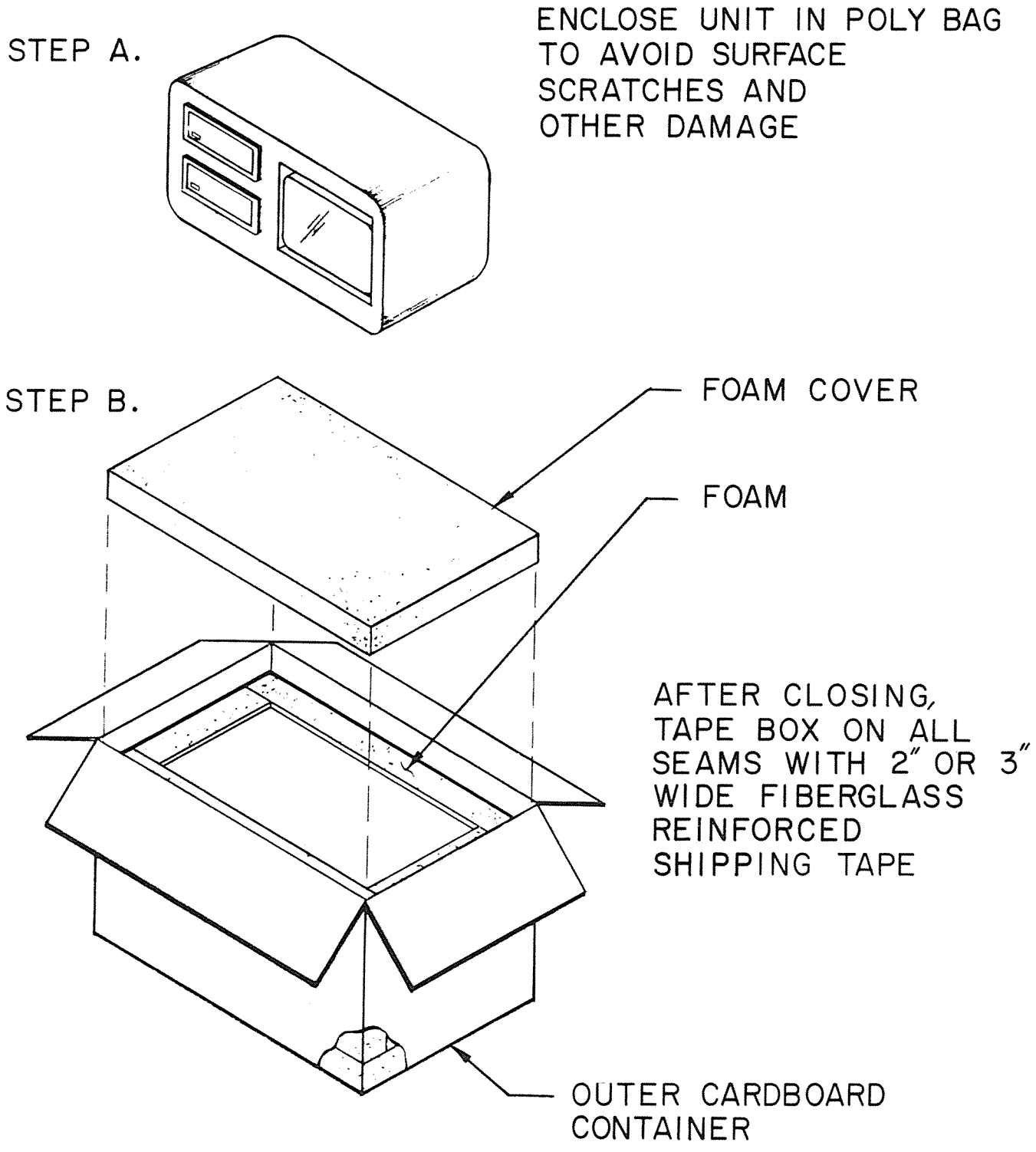
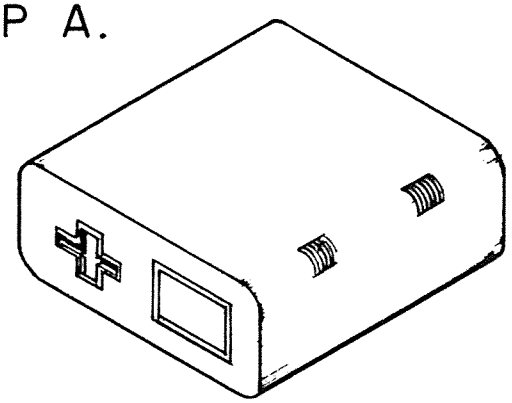


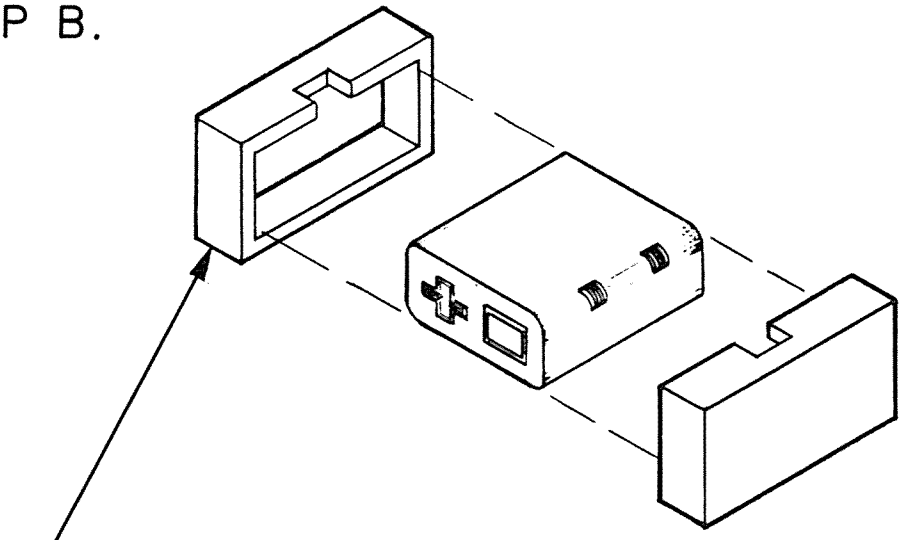
FIGURE 3-12
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 2

STEP A.



ENCLOSE UNIT IN POLY BAG TO AVOID SURFACE SCRATCHES AND OTHER DAMAGE

STEP B.



MOLDED POLYURETHANE "CLAMSHELL" TO "CUBE" UNIT

FIGURE 3-13
RECOMMENDED SHIPPING PACK DESIGN, CONFIGURATION 3

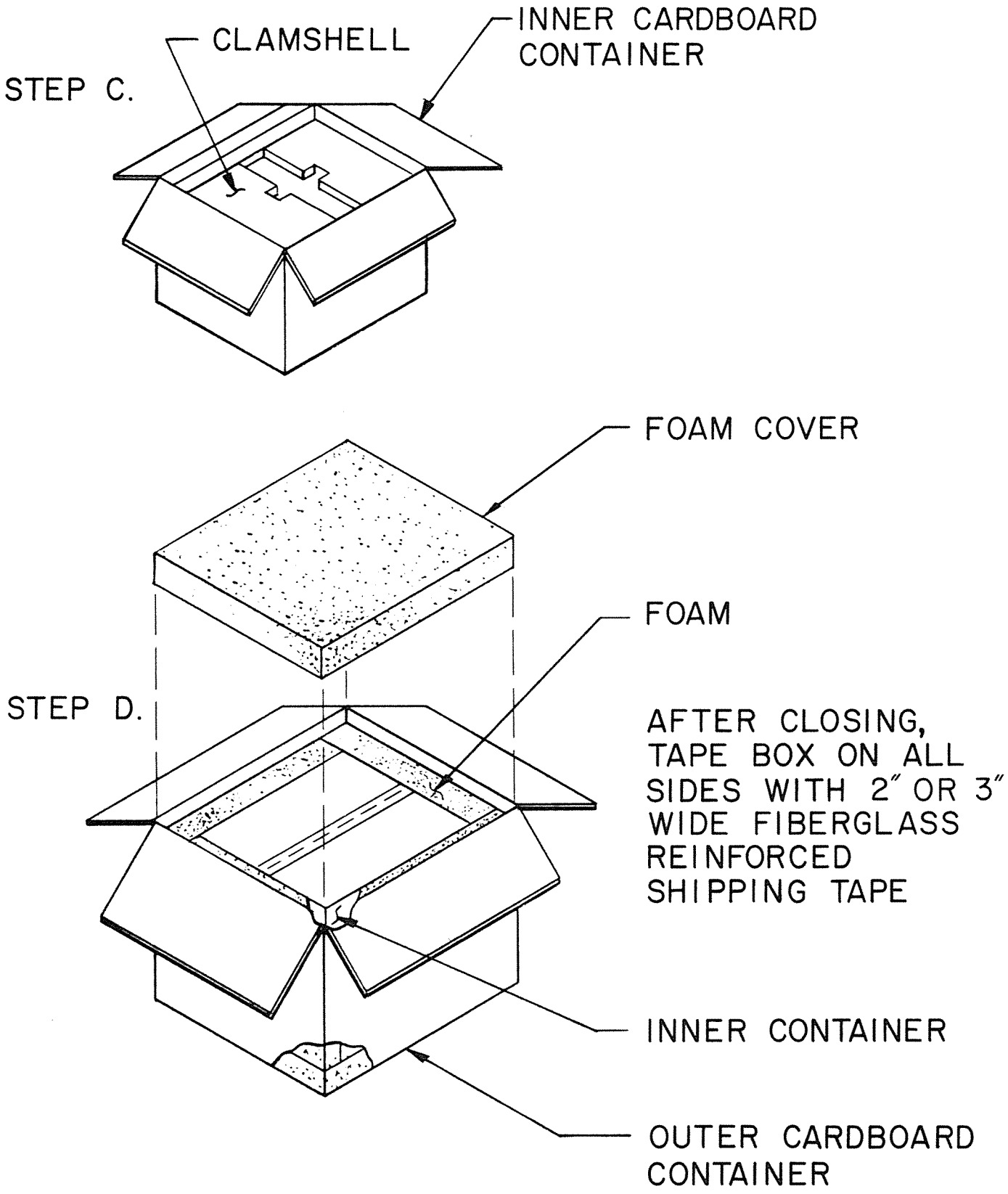
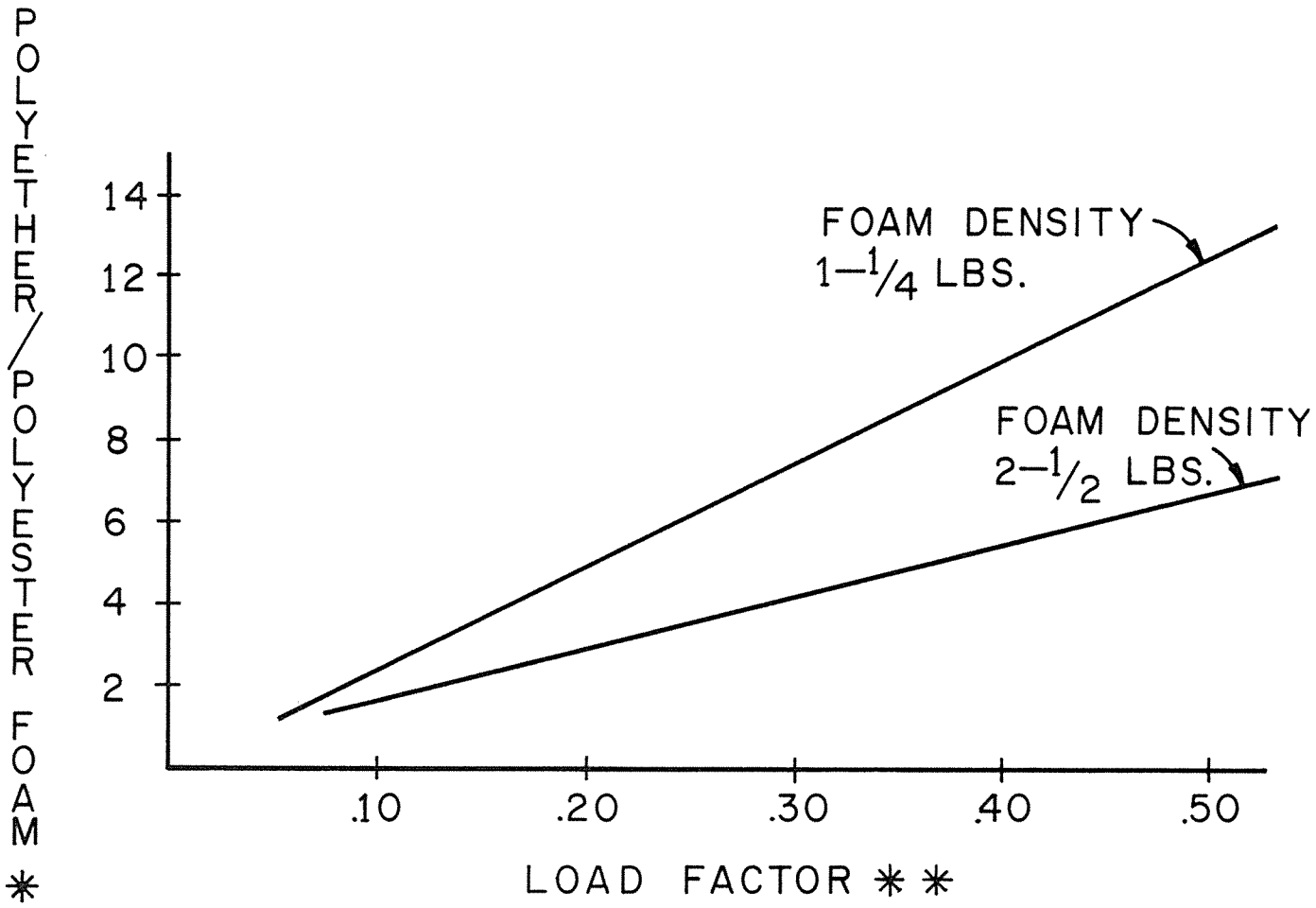


FIGURE 3-13 (CONTINUED)
RECOMMENDED SHIPPING PACK DESIGN
CONFIGURATION 3



NOTE

THE GRAPH GIVES FOAM THICKNESSES TO SATISFY 10 G MINIMUM SHOCK LOADS ON STANDARD 30 INCH DROP TEST. HENCE, ALL PACKAGE DESIGNS SHOULD BE TESTED TO VERIFY THEIR ULTIMATE PERFORMANCE.

* THICKNESS IS IN INCHES.

**THE LOAD FACTOR IS IN LBS. PER SQ. INCH.

THE FORMULA IS : $\text{LOAD FACTOR} = \dfrac{\text{UNIT'S WEIGHT (LBS.)}}{\text{SMALLEST SIDE OF UNIT (SQ. INCHES)}}$

FIGURE 3-14
LOAD GRAPH

SECTION 4

TROUBLESHOOTING GUIDE AND REPLACEMENT PROCEDURE

INTRODUCTION

This section is designed to help locate and correct failures related to the drive. Table 4-2 is a troubleshooting guide outlining the problem, its possible cause, and the recommended action. This section also contains parts removal, replacement, and adjustment procedures.

In all cases, the power supply voltages should be checked before proceeding.

4.1 TROUBLESHOOTING GUIDE

TEST EQUIPMENT

The following test equipment, or its equivalent, is recommended:

1. Oscilloscope, Tektronix 465—vertical and horizontal sensitivity plus three percent specified accuracy—with three 10X probes, each with individual ground leads.
2. Counter Timer, Monsanto Model 100B.
3. Digital Voltmeter (DVM), John Fluke Model 800A.

TEST POINTS

Table 4-1 contains each test point by function name. All test points referred to are on the logic board. Figure 4-1 illustrates their locations.

TABLE 4-1
TEST POINTS

Test Point	Signal
1, 4, 9, 11, 12, 13, 16, 17	Logic Ground
2	Direction
3	Index
5	Photo Sensor, Track 0
6	Track 0
7	Step
8	Seek Complete
10	Pulse Read Data
14	− Analog Read Data
15	+ Analog Read Data
18	Reserved +5 volts D. C.
19	Cable Detect +5 volts D. C.

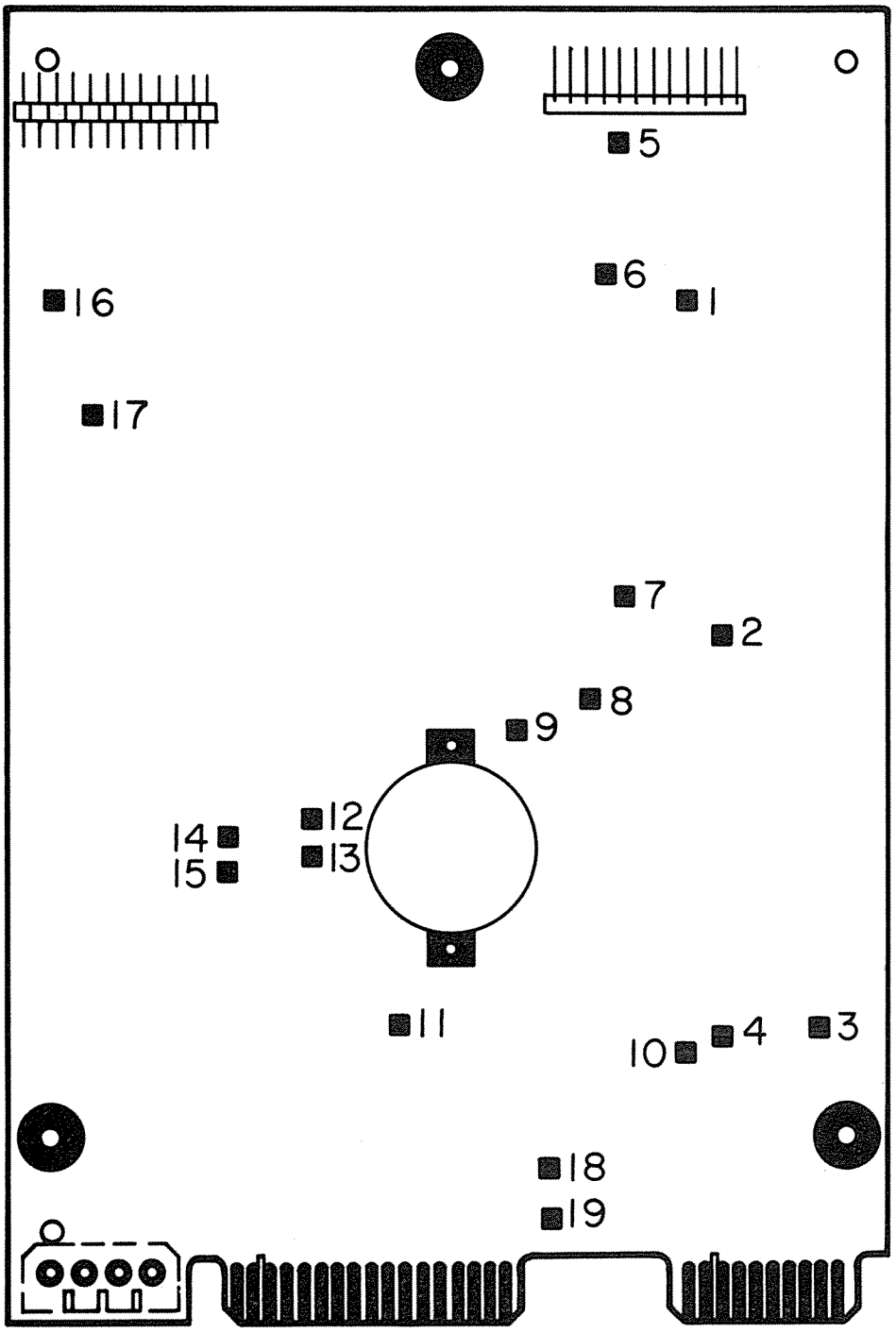


FIGURE 4-1
TEST POINT LOCATIONS

TABLE 4-2
TROUBLESHOOTING GUIDE

Problem	Possible Cause	Recommended Action
No activity lamp.	Not selected.	Check for correct drive select jumper.
	Lamp not plugged in.	Check Connector P-7.
	Lamp faulty.	Replace lamp.
	Logic board faulty.	Replace logic board.
No index.	Not selected.	Check drive select jumper.
	Index sensor not plugged in.	Check Connector P-5
	Index sensor misadjusted.	Readjust Index sensor.
	Index sensor faulty.	Replace sensor.
	Logic board faulty.	Replace logic board.
No Track 0.	Not selected.	Check drive select jumper.
	Track 0 sensor not plugged in.	Check Connector P-9.
	Track 0 sensor misadjusted.	Readjust Track 0 sensor.
	Track 0 sensor faulty.	Replace Track 0 sensor.
	Logic board faulty.	Replace logic board.
Drive not ready.	Not selected.	Check drive select jumper.
	No index.	See "No index."
	No Track 0.	See "No Track 0."
	Motor not up to speed or not turning.	See "Motor not up to speed, not turning."
	Drive does not seek. Drive does not restore.	See "Drive does not seek or restore."

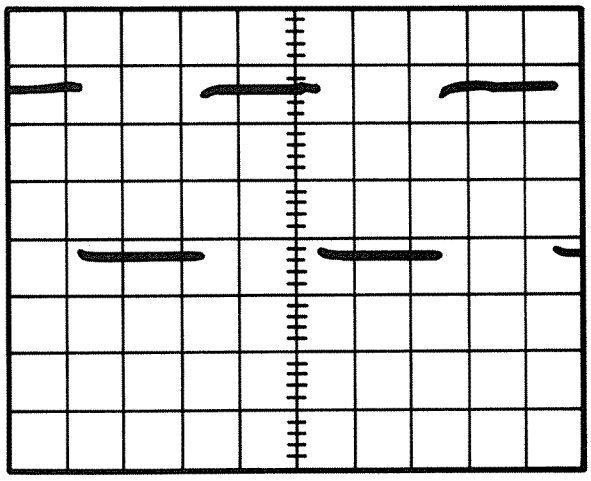
TABLE 4-2 (CONTINUED)
TROUBLESHOOTING GUIDE

Problem	Possible Cause	Recommended Action
Drive does not seek or restore.	Drive not selected.	Check drive select jumper.
	Stepper motor not plugged in.	Check Connector P-8.
	Logic board faulty.	Replace logic board.
	Spindle motor speed misadjusted.	Readjust spindle motor's speed.
	Stepper motor faulty.	Return to factory for repair.
	Foreign object interfering with positioning arm or damper.	Remove foreign object.
Motor not up to speed, not turning.	Spindle circuit board not plugged in.	Check Connector P-12.
	Spindle motor not plugged in.	Check Connectors P-10 and P-11.
	Faulty Spindle circuit board (see Figure 4-2).	Replace circuit board.
	Motor not up to speed.	Adjust spindle speed.
	Motor faulty.	Return to factory for repair.
	Brake misadjusted.	Readjust brake.
Does not read.	Not selected.	Check drive select jumper.
	Heads not selected.	Check head select interface lines.
		Check jumper 3P W13, installed for Model Number TM503 (see Table 3-2, page 3-10).
	Head cable not plugged in.	Check Connector P-6.
	Logic board faulty (see Figure 4-3).	Replace logic board.
	Defective head.	Return to factory for repair.

TABLE 4-2 (CONTINUED)
TROUBLESHOOTING GUIDE

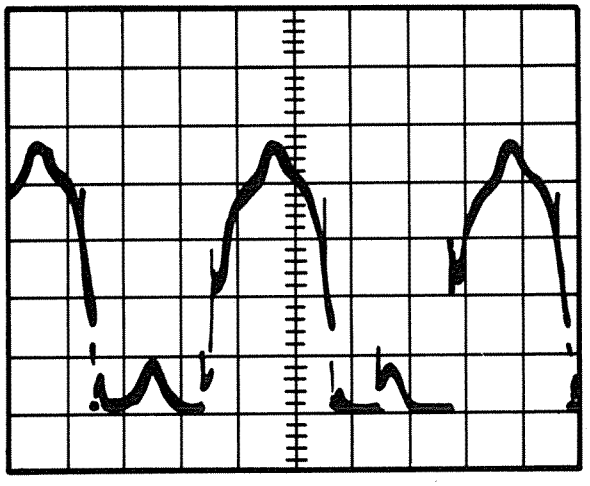
Problem	Possible Cause	Recommended Action
Does not read.	Improper position.	See "Drive does not seek or restore."
	Drive not ready.	See "Drive not ready."
Does not write.	No Write Gate for writing.	Check Write Gate interface line.
	Not selected.	Check drive select jumper.
	Heads not selected.	See "Does not read."
	Head cable not plugged in.	Check Connector P-6.
	Logic board faulty.	Replace logic board.
	Defective head.	Return to factory for repair.
	Drive not ready.	See "Drive not ready."

VOLTAGE SCALE
2 VOLTS PER DIVISION



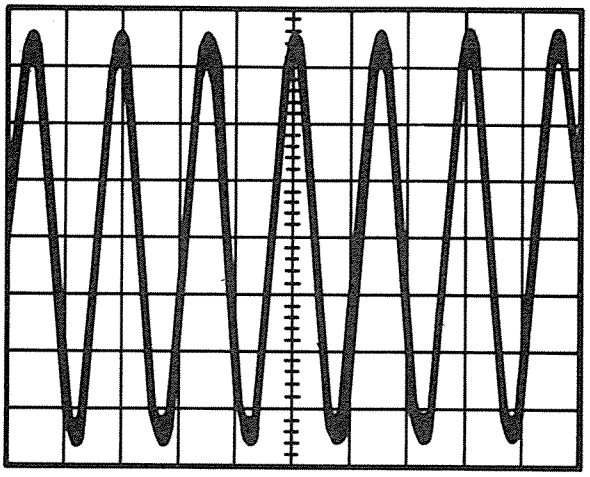
TIME SCALE: 2 MILLISECONDS PER DIVISION
HALL SENSE
LOCATION P10-1

VOLTAGE SCALE
5 VOLTS PER DIVISION

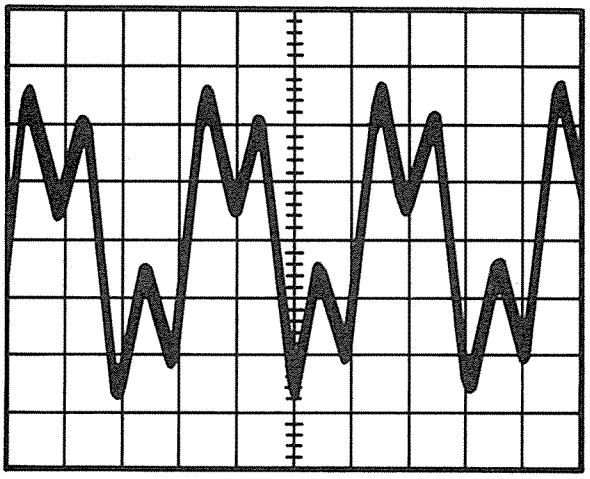


TIME SCALE: 2 MILLISECONDS PER DIVISION
SPINDLE MOTOR WINDINGS
LOCATION P10-6

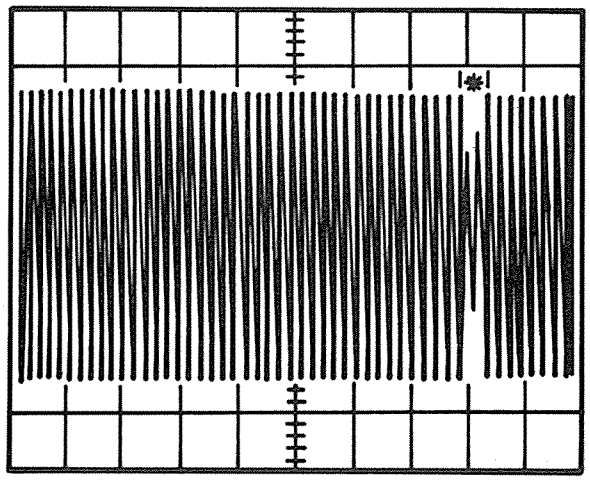
FIGURE 4-2
SPINDLE MOTOR CIRCUIT BOARD WAVEFORMS



ALL ZERO PATTERN



ALTERNATING ONES AND ZEROS



*BIT DROPOUT CAUSED BY MEDIA DEFECT

FIGURE 4-3
READ DATA WAVEFORMS 15 TPR + AND 14 TPR —

4.2 REPLACEMENT PROCEDURES

Do not rotate spindle motor or head positioning mechanism. Damage to heads and/or media may occur.

Remove power prior to replacing parts.

The following assemblies may be replaced:

Control and Data Circuit Board Assembly
Front Panel L.E.D. Assembly
Linear Brake Assembly
Front Panel
Index Assembly
Spindle Control Circuit Board Assembly
Frame Assembly
Track 0 Sensor Assembly

TOOLS REQUIRED

Number 2 Phillips screwdriver
3/16" nut driver
5/16" nut driver
.008" or .010" feeler gauge

CONTROL AND DATA CIRCUIT BOARD ASSEMBLY

REMOVAL

To remove the Control and Data Circuit Board Assembly:

1. Remove the three screws that attach the circuit board to the chassis.
2. Remove the Connectors J4 and J5 from the circuit board.
3. Slide the circuit board toward the side of the frame, lift up on the free side of it, and remove remaining connectors.

REPLACEMENT

To replace this assembly, reverse Steps 1 through 3.

FRONT PANEL L.E.D. ASSEMBLY

REMOVAL

To remove the Front Panel L.E.D. Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Remove the L.E.D. Assembly by pressing the center of the Front Panel L.E.D. Assembly with a blunt tool.

   NOTE
   Press from the inside to the outside of the panel.

3. Remove the square retainer from the assembly.

REPLACEMENT

To replace this assembly, reverse Steps 1 through 3.

LINEAR BRAKE ASSEMBLY

REMOVAL

To remove the Linear Brake Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Remove Connector J11 from the Spindle Control circuit board.
3. Remove the 5/16-inch nut and washer from the mounting stud.
4. Remove the Linear Brake Assembly.

REPLACEMENT

To replace the assembly, reverse Steps 1 through 4.

ADJUSTMENT

To adjust the Linear Brake Assembly:

1. Loosen the 5/16-inch mounting nut.
2. Set the feeler gauge, adjusted to 0.014 inches, between the brake pad and the spindle drive motor rotor.
3. Push the brake pad up against the feeler gauge.
4. Align the brake shoe with the Spindle Drive Motor rotor.
5. Tighten the 5/16-inch mounting nut.
6. Remove the feeler gauge.

INDEX ASSEMBLY

REMOVAL

To remove the Index Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Loosen the lock nut on the Index Assembly bracket.
3. Unscrew the Index Assembly, and remove.

REPLACEMENT

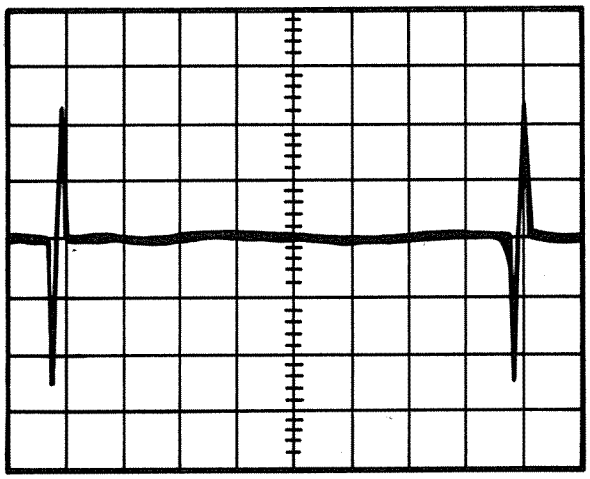
To replace the Index Assembly, reverse Steps 1 through 3.

ADJUSTMENT

To adjust the Index Assembly:

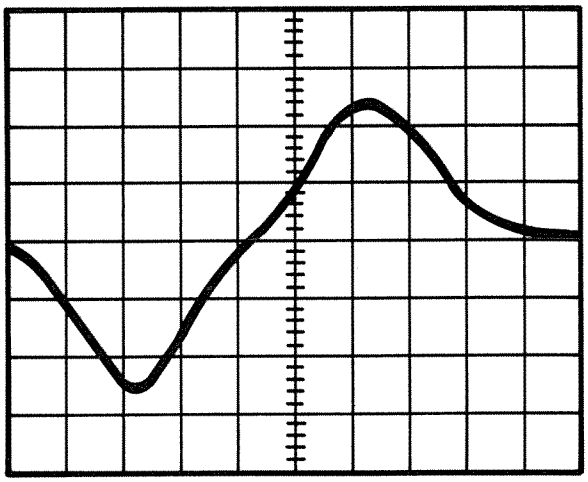
1. Loosen the 3/8-inch locking nut.
2. Adjust the Index Assembly to between 0.008 and 0.010 inches from the motor rotor.
3. Use a 100 megahertz or greater bandwidth oscilloscope.
4. Verify the A. C. signal as seen at U9, Pin 6, is greater than one volt peak to peak (see Figure 4-4).
5. There must not be more than 100 millivolts peak ripple on the base line.

VOLTAGE SCALE
1 VOLT PER DIVISION



TIME SCALE: 2 MILLISECONDS PER DIVISION
LOCATION U9-6

VOLTAGE SCALE
1 VOLT PER DIVISION



TIME SCALE: 50 MICROSECONDS PER DIVISION
LOCATION U9-6

FIGURE 4-4
INDEX SENSOR

FRONT PANEL

REMOVAL

To remove the front panel:

1. Wedge a taper shim 0.030 inch under the edge of the front panel.
2. Remove the front panel from the drive frame.
3. Clean the front panel thoroughly with solvent.

REPLACEMENT

To replace the front panel, apply new double back tape, and fit the panel over the drive frame.

SPINDLE CONTROL CIRCUIT BOARD ASSEMBLY

REMOVAL

To remove the Spindle Control Circuit Board Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Remove Connectors J10 and J11 from the Spindle Control circuit board.
3. Remove the three screws that attach the board to the chassis.
4. Lift the board straight up and out.

REPLACEMENT

To replace the board, reverse Steps 2 through 4. When replacing connectors, ensure the proper pin orientation.

ADJUSTMENT

To adjust the Spindle Control circuit board:

1. Set potentiometer R23 (closest to interface connectors, single turn) to its approximate center position.
2. Using a dual channel oscilloscope, connect one channel to R26 (resistor lead closest to the power transistor leads on Spindle Control Circuit Board), and set scope to 100 millivolts per division. Connect the other channel of the scope to test point three on the logic board (index), and set the voltage scale at one volt per division and the time base at two milliseconds per division.
3. Apply power to the drive and wait 15 seconds for the spindle motor to come up to speed.
4. While the scope is triggered on index, adjust the speed control potentiometer R5 on the spindle control board (10 turn pot closest to the front of the drive), so the time between index pulses is between 16 and 17 milliseconds.
5. Trigger the scope to the line frequency (60 Hertz). Adjust R5 so index pulses are stationary on the scope screen.
6. Adjust R23 so voltage spikes, both positive and negative going, across R26 are minimal (see Figure 4-5).
7. Repeat Steps 5 and 6 until no further improvement can be made.

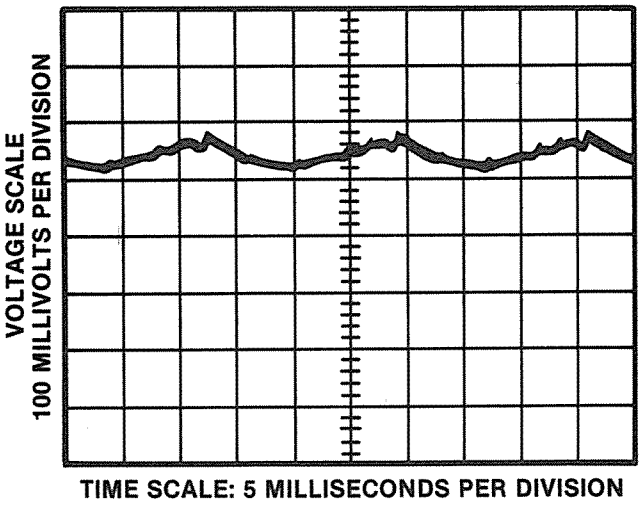


FIGURE 4-5
VOLTAGE SPIKES

FRAME ASSEMBLY

REMOVAL

To remove the Frame Assembly:

1. Remove the Control and Data circuit board.
2. Remove the Spindle Control circuit board.
3. Remove the three frame nuts and the six washers.
4. Remove the Frame Assembly.

REPLACEMENT

To replace the Frame Assembly, reverse Steps 1 through 4 above.

TRACK 0 SENSOR ASSEMBLY

Do not move the positioning mechanism or Track 0 stop.

REMOVAL

To remove the Track 0 Sensor Assembly:

1. Remove the Circuit Board Assembly.
2. Loosen the screw on the Track 0 Sensor Assembly mount.
3. Swing the mount clear, and remove the screw that holds the Track 0 Sensor Assembly.

REPLACEMENT

To replace the Track 0 Sensor Assembly, reverse Steps 1 through 3 above.

ADJUSTMENT

To adjust the Track 0 Sensor Assembly:

1. Loosen the screw.
2. Adjust the sensor so that it is 2.5 $\pm$1 volt at Test Point 5, while stepping out from Track 5 to Track 0, and the positioner is on Track 2 plus or minus one track.
3. Verify that Test Point 6 changes logic level at Track 2, plus or minus one track (see Figure 4-6).

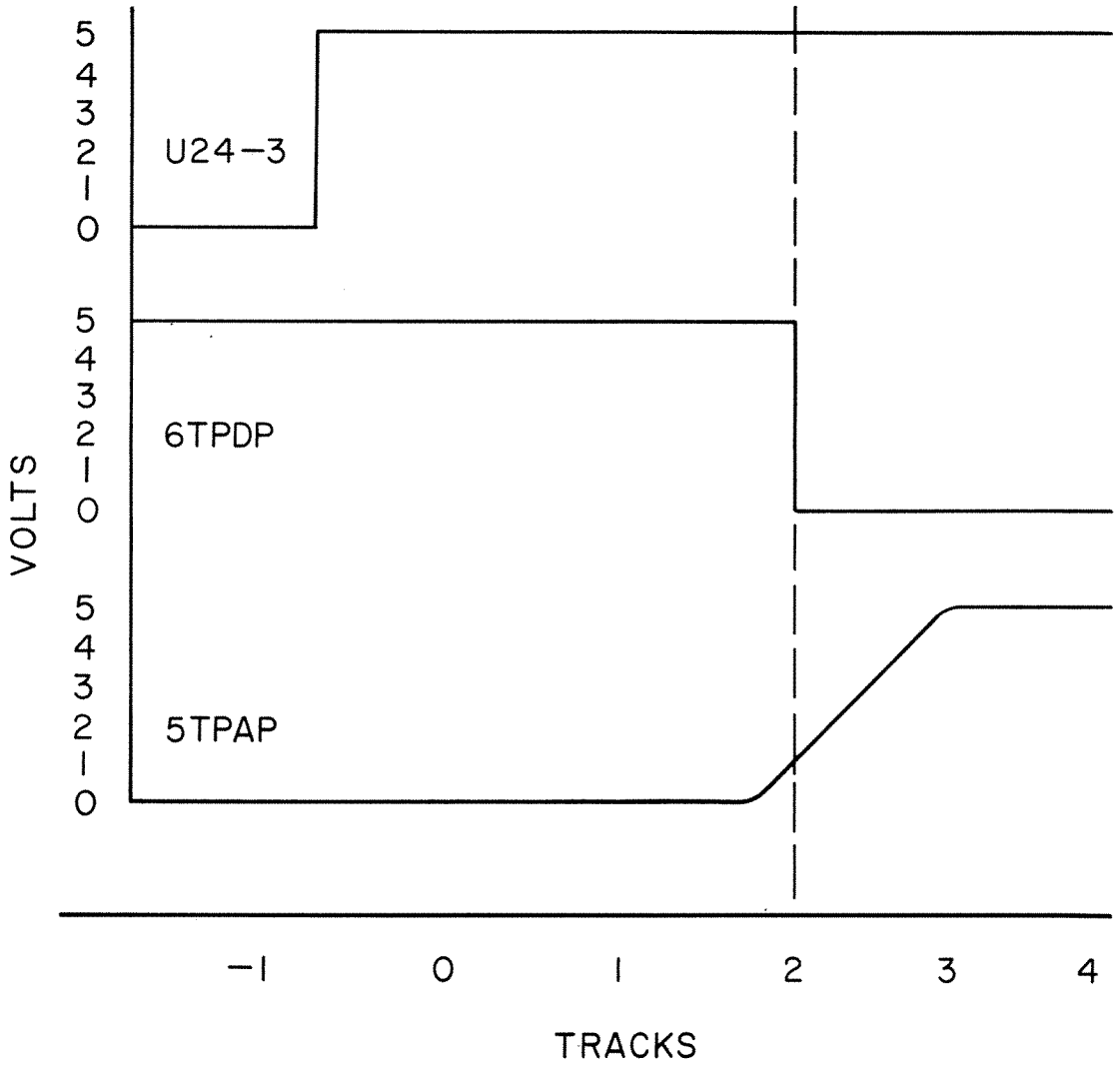


FIGURE 4-6
TRACK 0 ADJUSTMENT

APPENDIX A

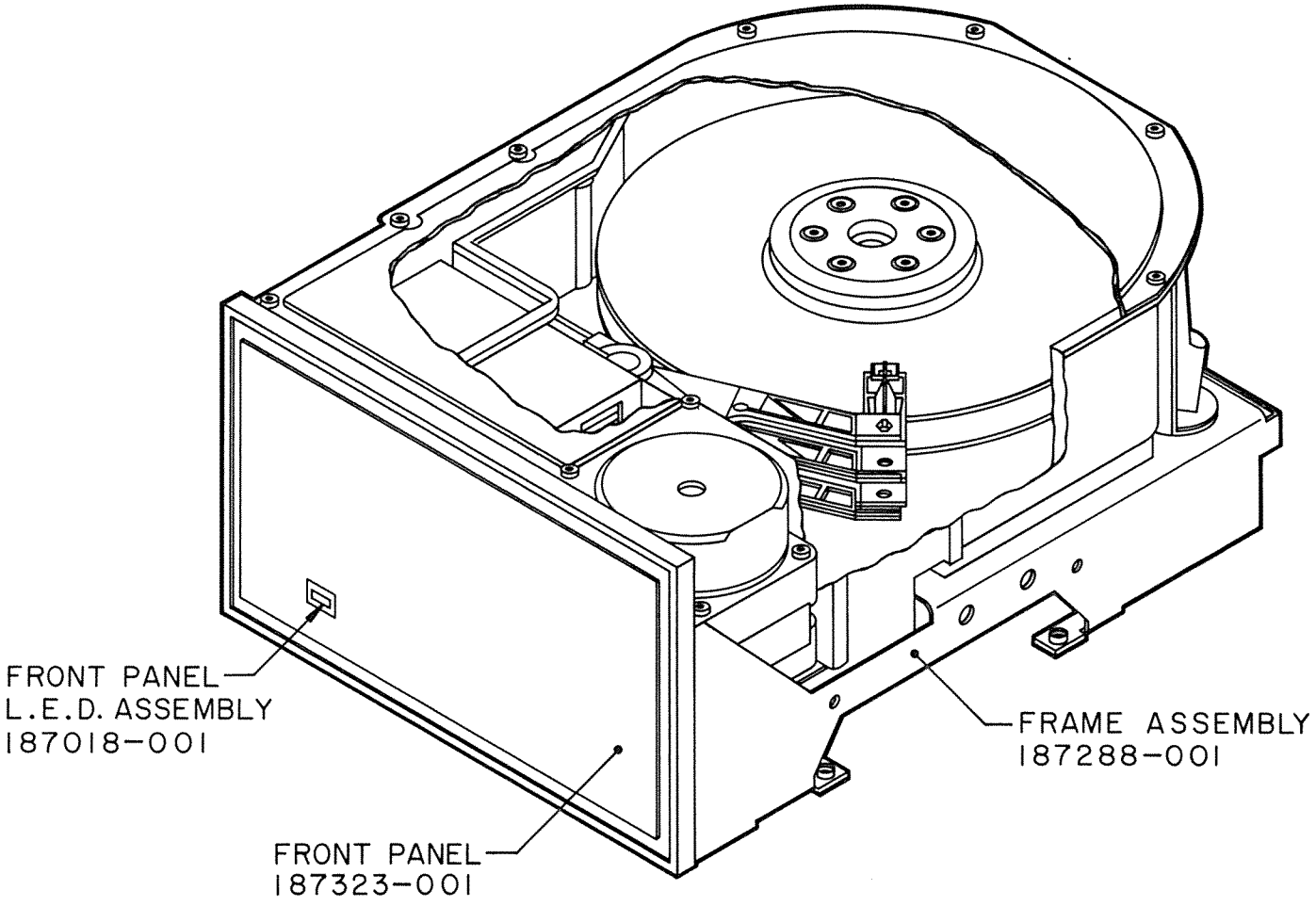
RECOMMENDED SPARE PARTS LIST AND MAJOR ASSEMBLIES

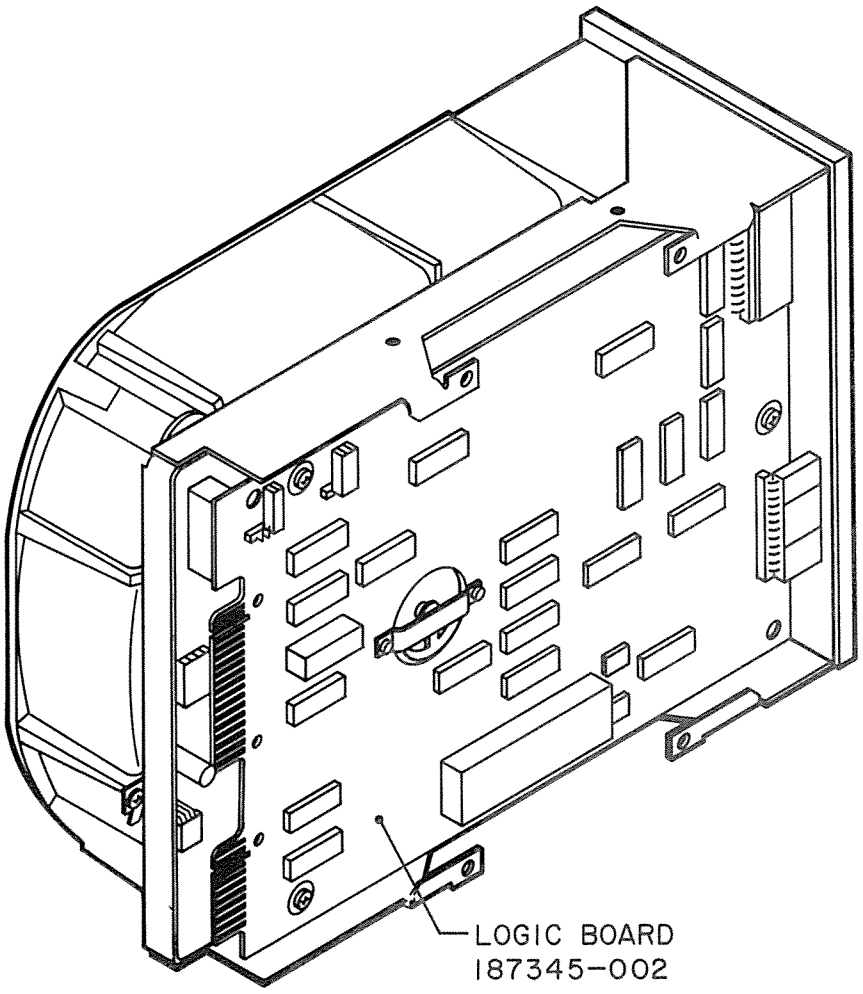
All assemblies with part numbers are available for purchase as spare replacement parts. The items without alpha designators on the drawings are for reference only, and cannot be purchased as spare replacement parts.

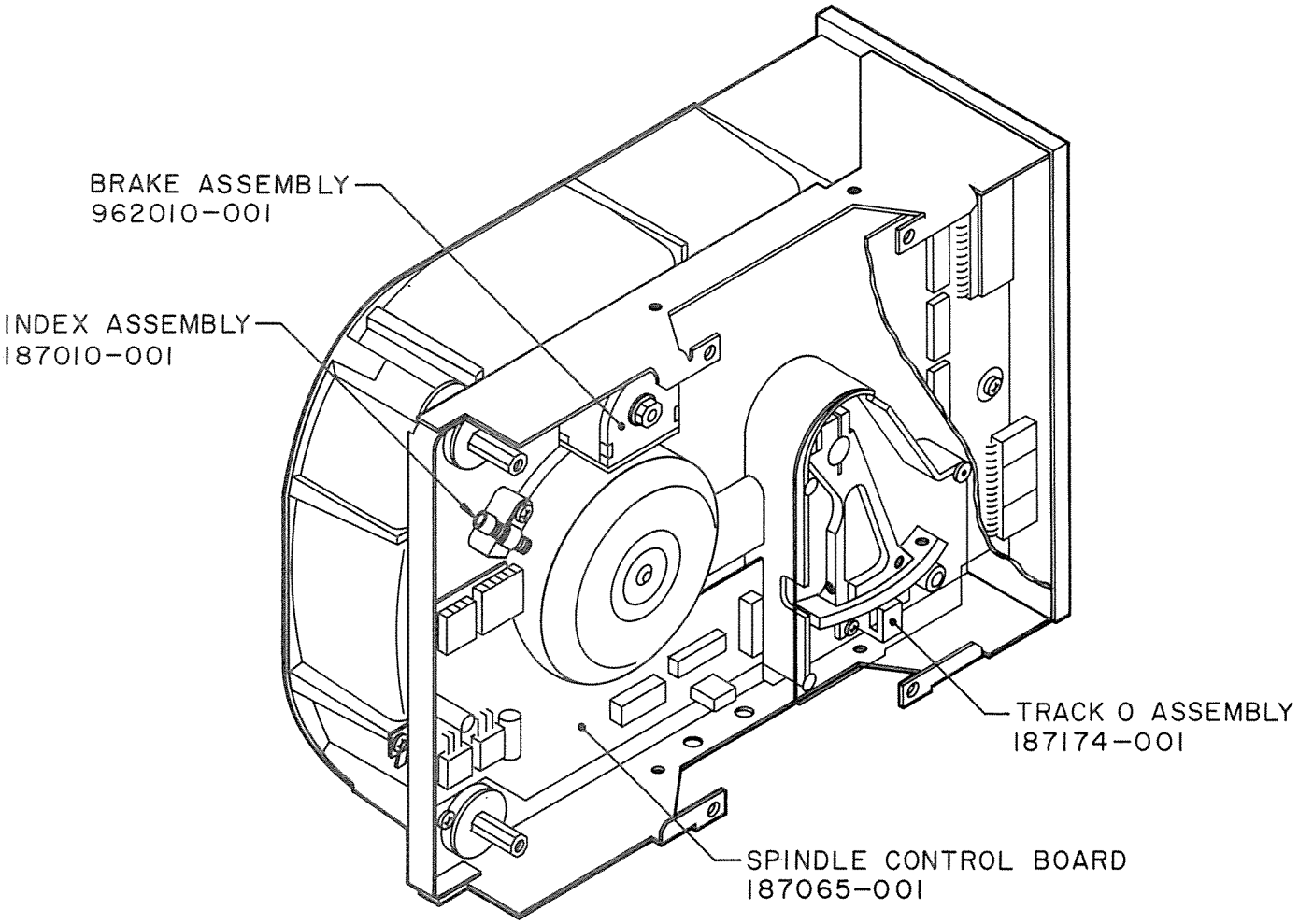
If an assembly has been determined faulty, and is not listed as a spare replacement, the drive must be returned to the manufacturer for repair.

RECOMMENDED SPARE PARTS LIST

Description	Part Number
Brake Assembly	962010-001
Index Assembly	187010-001
Track 0 Assembly	187174-001
Frame Assembly	187288-001
Front Panel	187323-001
Spindle Control Board	187065-001
Logic Board	187345-002
Front Panel L.E.D. Assembly	187018-001
Single Pack Shipping Container	187125-001 (Not Shown)
Four Pack Shipping Container	187125-002 (Not Shown)


FRONT PANEL
L.E.D. ASSEMBLY
187018-001
FRONT PANEL
187323-001
FRAME ASSEMBLY
187288-001

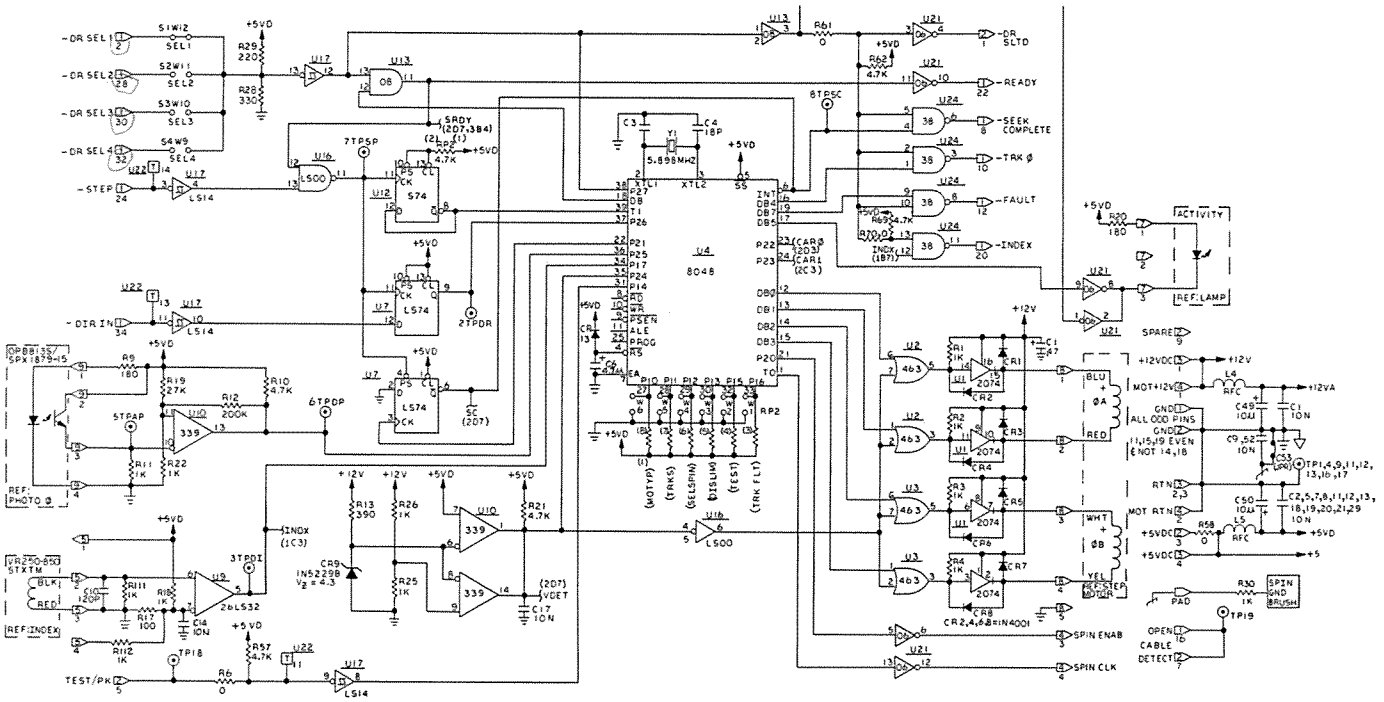

LOGIC BOARD
187345-002


BRAKE ASSEMBLY
962010-001
INDEX ASSEMBLY
187010-001
TRACK 0 ASSEMBLY
187174-001
SPINDLE CONTROL BOARD
187065-001

APPENDIX B

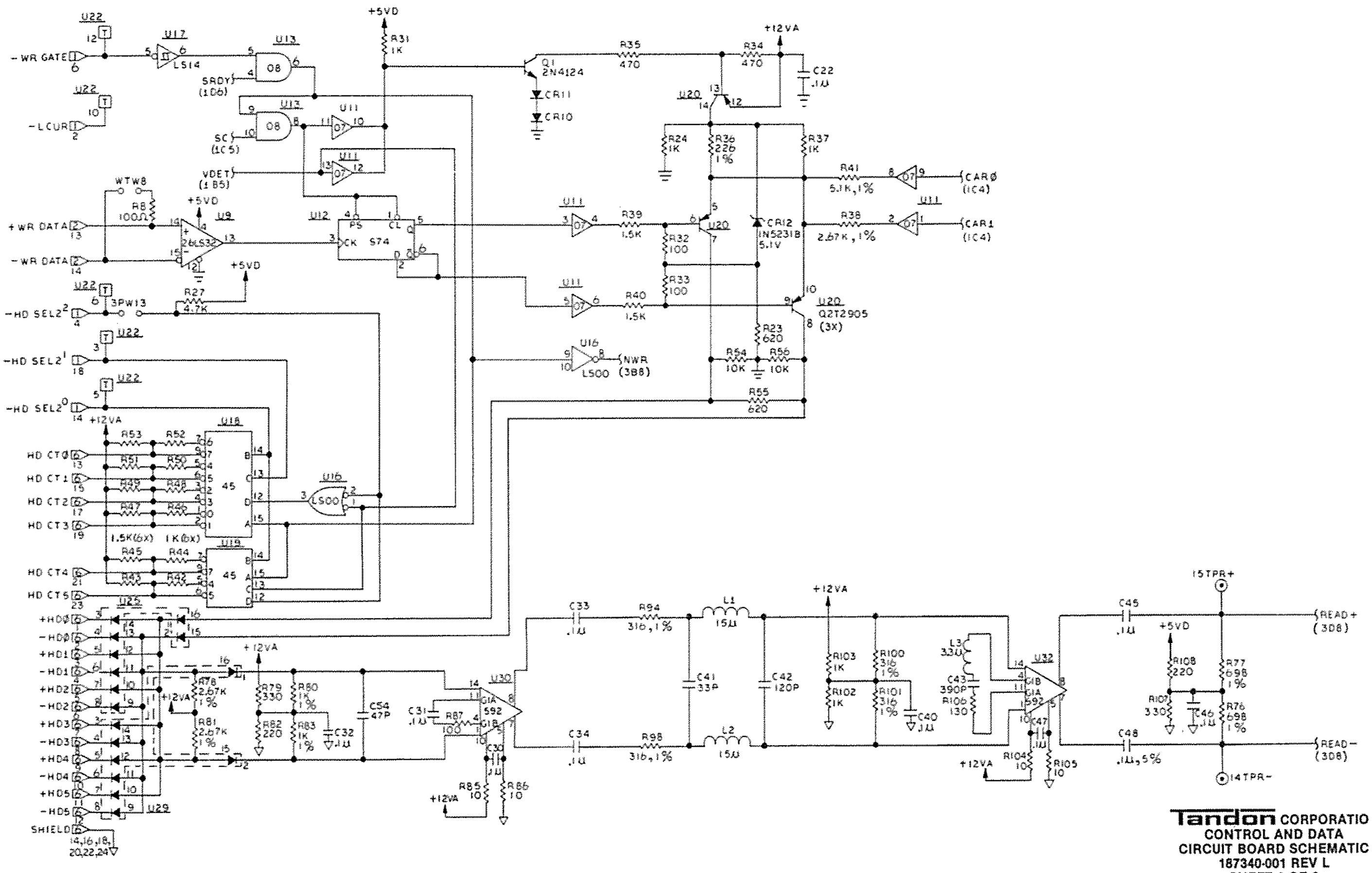
CIRCUIT BOARD SCHEMATICS AND ASSEMBLY DRAWINGS

This appendix contains the current circuit board schematics and assembly drawings for the TM500 series of disk drives.

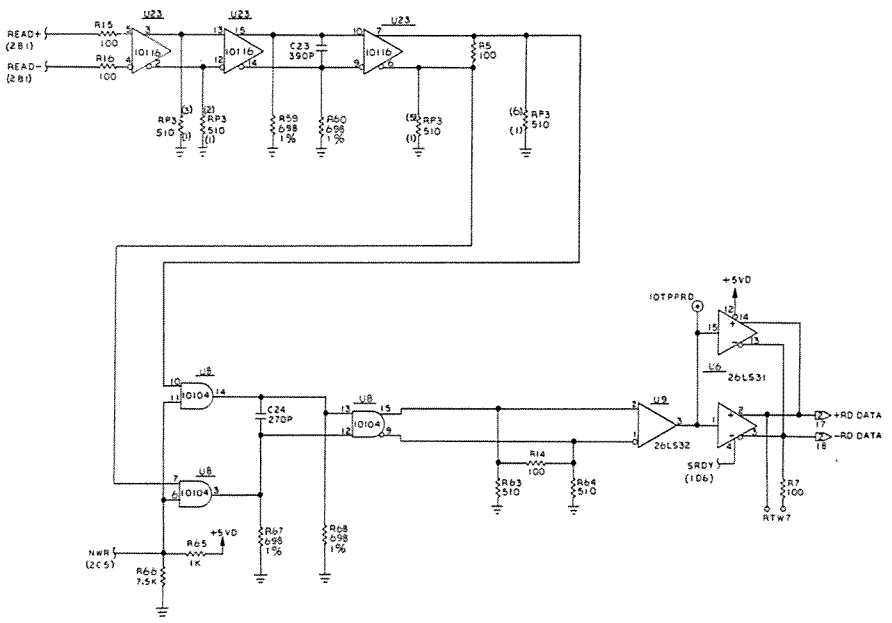


. Y DENOTES CONNECTOR JX, PIN Y.
. INDUCTORS ARE IN UH, 10%.
. DIODES ARE IN4446 OR EQUIV.
. CAPS ARE IN PF, NF, OR UF, 25V MIN. TOLERANCE IS 10% FOR VALUES ABOVE 1N, 5% OTHERWISE.
. 1% RESISTORS ARE 1/8W.
. RESISTORS ARE IN OHMS, 1/4W 5%.
9. UNVALUED COMPONENTS ARE OMITTED.
8. X DENOTES PIN X OF (U22) TERM PAK. = 220 330 X
7. DENOTES TEST POINT.

Tandon CORPORATION
CONTROL AND DATA
CIRCUIT BOARD SCHEMATIC
187340-001 REV L
SHEET 1 OF 3



Tandon CORPORATIO
CONTROL AND DATA
CIRCUIT BOARD SCHEMATIC
187340-001 REV L
SHEET 2 OF 3



I.C. LOCATION AND VOLTAGE CHART					
LOCATION	TYPE	+5	+12	GND	UNUSED
U16	74LS00	14		7	
U21	7406	14		7	
U11	7407	14		7	
U13	7408	14		7	
U17	74LS14	14		7	1/6
U24	7438	14		7	
U18,U19	7445	16		8	
U7	74LS74	14		7	
U12	74S74	14		7	
U10	339		3	12	1/4
U2,U3	463	8		4	
U30,U32	592		NOTED	NOTED	
U1	UNL2074		NOTED	4,5,12,13	
U6	26LS31	16		8	2/4
U9	26LS32	16		8	1/4
U25,U29	2719				
U20	Q2T2905		NOTED		1/4
U4	8048	26,40		20	
U8	10104	1,16		8	1/4
U23	10116	1,16		8	
U14					
U22	TERM PAK	16		7,8	4/12

SHUNT PLUG PROGRAMMING			
W1-W13 SHUNT	FUNCTION	FACTORY PROGRAMMED	USAGE
W1	TRK FAULT	O	INSTALL FOR EXCESS TRK FAULT
W2	TEST	O	INSTALL FOR FACTORY TEST
W3	DISABLE LIMIT	O	INSTALL TO DISABLE SOFT LIMITS
W4	SPIN SELECT	O	INSTALL FOR SPIN SELECT
W5	TRACKS	S	INSTALL FOR 5 VERSION ONLY
W6	MOTOR TYPE	-	INSTALL FOR TYPE 1B MOTOR
RTW7	READ TERMINATOR	I	CLOSE ONLY@END DRIVE OF DAISY CHAIN DATA
WTW8	WRITE TERMINATOR	I	CLOSED FOR RADIAL DATA
S4W9	DRIVE SELECT 4	O	INSTALL 1 OF 4 PLUGS ONLY
S3W10	DRIVE SELECT 3	O	PLUG CORRESPONDS TO
S2W11	DRIVE SELECT 2	O	DRIVE ADDRESS
S1W12	DRIVE SELECT 1	I	
3PW13	3 DISC	603	CLOSE FOR MODEL 603 ONLY
U22	TERMINATOR PAK	I	INSTALL IN END DRIVE OF DAISY CHAIN
O = OMIT I = INSTALL			S = CLOSE FOR 5 VERSION ONLY 603 = CLOSE FOR TM603 ONLY

REFERENCE DESIGNATORS	
LAST USED	UNUSED
C54	C15,25-28,35-39,44,51
CR13	
J9	
L5	
Q1	
R111	R71THRU75,84,86,93,95-97,99,106,110
RP3	RP1
TP19	
U32	U5,14,15,20-28,31
W13	
Y1	

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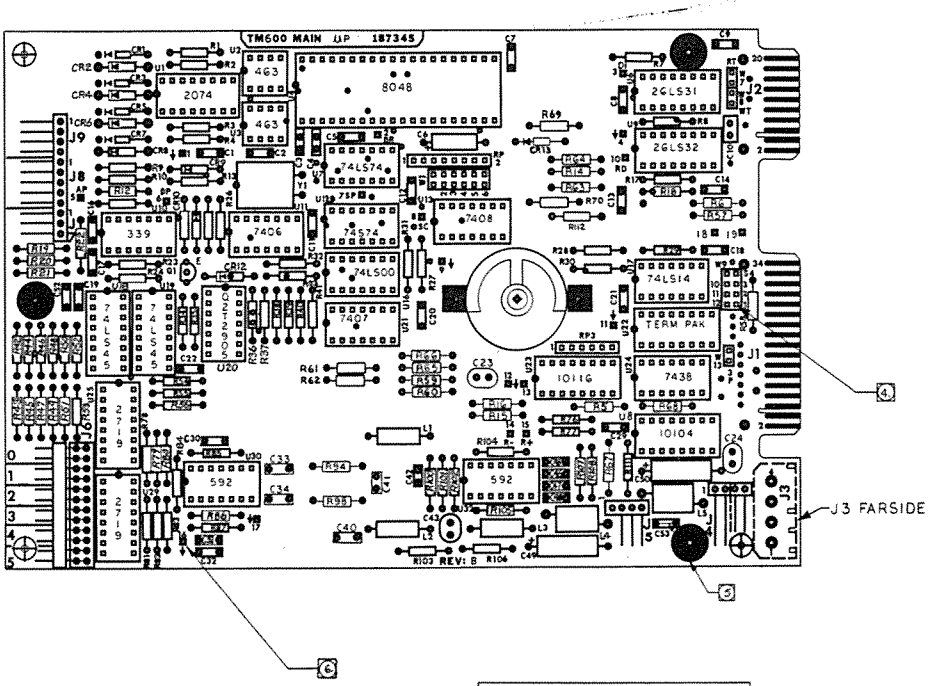
CONTROL AND DATA
CIRCUIT BOARD SCHEMATIC
187340-001 REV L
SHEET 3 OF 3



6. T.P. WIRE TO EXTEND .25 MIN, .30 MAX ABOVE COMPONENT SIDE OF P.C. BOARD 19 PLACES.

5. SOLDER #24AWG UNINSULATED TIN COATED SOLID COPPER WIRE MAY SUBSTITUTE 1/4W RESISTOR LEAD WIRE.

4. .025 SQ. SHUNT JUMPER POSTS (W1-W13) TO BE INSTALLED ⊥ TO BOARD SURFACE WITH FLATS TO BE || TO BOARD EDGES, 26 PLACES.

3. SOLDER #24 AWG UNINSULATED TIN COATED SOLID COPPER WIRE MAY SUBSTITUTE 1/4 W RESISTOR LEAD WIRE.

2. REF. DOCUMENT: 187340-001-CIRCUIT SCHEMATIC
187341-001 ARTWORK

1. SEE SHEET 1 THRU 3 FOR PART LIST.

REFERENCE DESIGNATORS	
LAST USED	UNUSED
C53	C15,25-28,35-39,44,51
CR13	
J9	
L5	
Q1	
R111	R71 THRU 75,88,93,95-97,99,109,110
RP3	RP1
TP19	
U32	U5,14,15,26-28,31
W13	
Y1	

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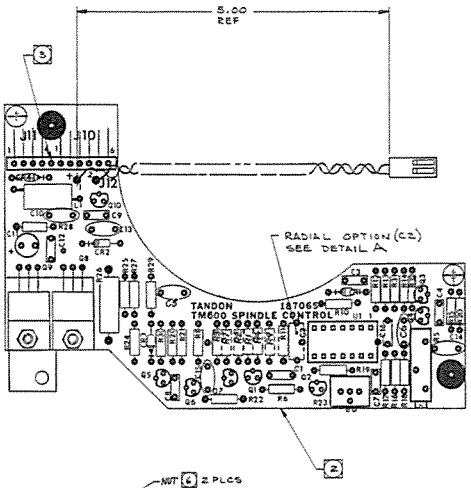
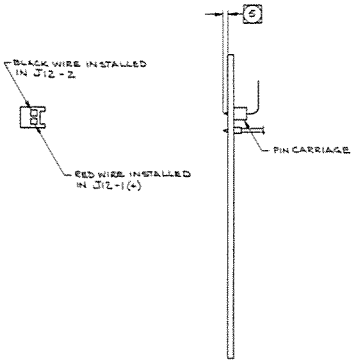
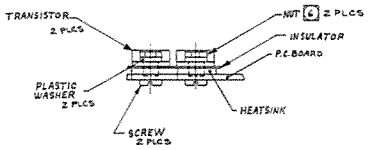
CONTROL AND DATA
CIRCUIT BOARD ASSEMBLY
187345-001 REV S
SHEET 1 OF 1







7. REF DOCUMENT: 187060-001 CIRCUIT SCHEMATIC
187061-001 ARTWORK

[6] TORQUE 4.5 INCH LBS NOMINAL.

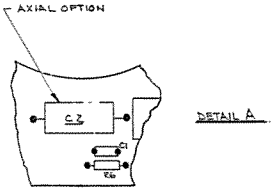
[5] MAX LENGTH OF COMPONT LEADS BELOW SOLDER SIDE BOARD AFTER ASSEMBLY & TRIMMING SHALL NOT EXCEED .08 INCH.

4. COMPONENT HEIGHT EXCEPT C11, SHALL NOT EXCEED .45 INCH ABOVE BOARD. CAPACITOR C11, NOT TO EXCEED .50 INCH ABOVE BOARD.

[3] CUT PIN TANGENT TO PIN CARRIAGE.

[2] THIS ASSEMBLY SHALL BE MADE FROM P.C.B. DETAIL 187060-001.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.



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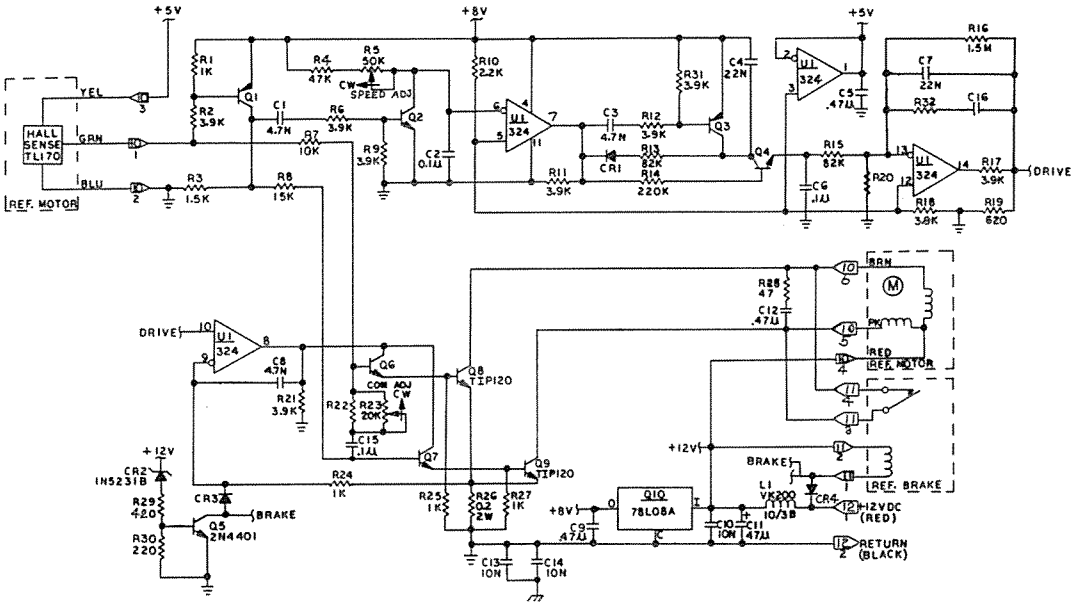
SPINDLE CONTROL
CIRCUIT BOARD ASSEMBLY
187065-001 REV J
SHEET 1 OF 1



7. UNVALUED COMPONENTS ARE OMITTED.
6. Y OR Y DENOTES CONNECTOR X, PIN Y.
5. PNP TRANSISTORS ARE 2N4125.
4. NPN TRANSISTORS ARE 2N4124.
3. DIODES ARE 1N4446 OR EQUIV.
2. CAPACITORS ARE 25V, 10%, PF, NF, OR UF.
1. RESISTORS ARE IN OHMS, 1/4 W, 5%.

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SPINDLE CONTROL
CIRCUIT BOARD SCHEMATIC
187060-001 REV E
SHEET 1 OF 1

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