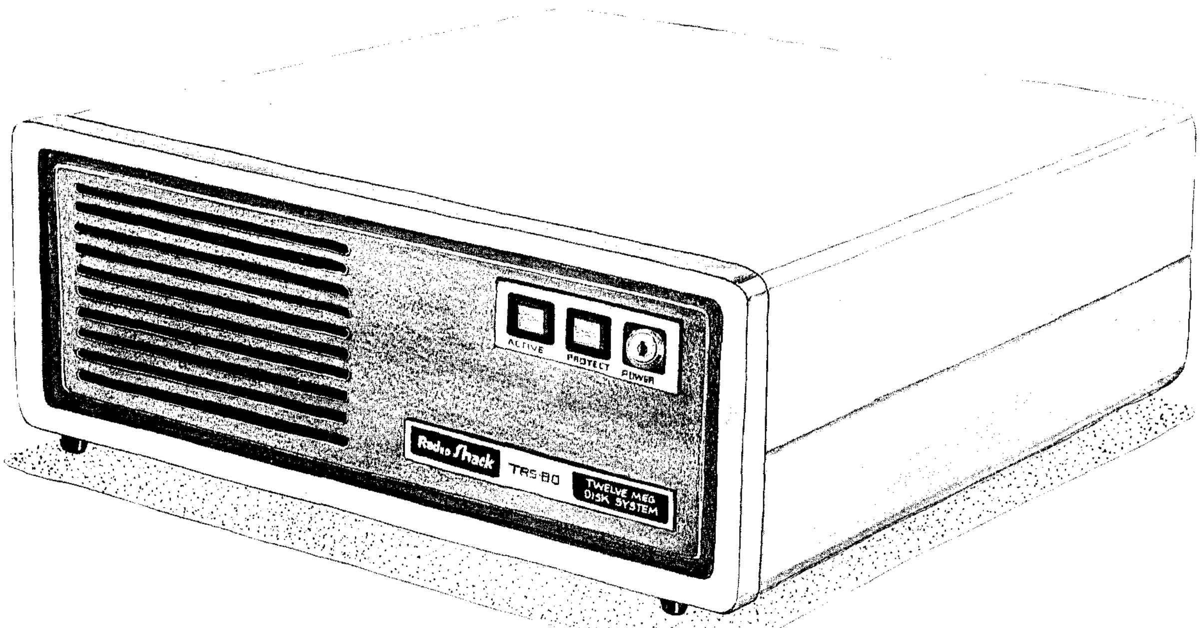
Radio Shack®

Service Manual

TRS-80®

Twelve-Meg Hard Disk

Catalog Number 26-4152/3



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TRS-80® 12-Meg Hard Disk

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Catalog Number 26-4152

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Contents

****
Warnings
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Do not move or tilt the Hard Disk Drive unit while the drive is running. Permanent damage to the drive may occur resulting in the loss of information or damage to the disk.

Do not drop the Hard Disk Drive unit from any height as permanent damage to the drive may occur.

1/ Overview

The TRS-80 12-Meg Hard Disk Unit consists of three non-removable 5.25-inch disks. There are six Read/Write heads (one on each side of each platter) which move towards or away from the center of the disk as needed.

The Disks and Read/Write heads are fully enclosed in a sealed chamber. A special air filteration system prevents dust and other particles, which destroy data, from reaching the disks. Another filtering system allows pressure equalization with the "outside" air pressure.

UNDER NO CIRCUMSTANCES MUST THE CHAMBER BE UNSEALED IN THE FIELD. A CLASS 100 CLEAN ROOM ENVIRONMENT IS NEEDED FOR UNDER-THE-BUBBLE REPAIR.

On all Hard Disk Units, flaws in the media are indentified at the factory before the disk drives are delivered to the customer. Attached to the bottom of each disk drive unit is a "Media Error Map". This map identifies the flawed tracks on that particular unit.

2/ Technical Specifications

Basically, the hard disk unit consists of three platters (or disks) lying parallel within the unit. There are also six Read/Write heads, one on each side of each platter. These heads move towards or away from the center of the disk as needed.

When a unit is purchased, there will be no more than 3 tracks per head with defects. This will not exceed 8 tracks per drive with defects. Also there will not be any flaws on Track 0.

Disks/Platters	3
Heads/Recording Surfaces	6
Tracks per Inch	254
Cylinders	230
Tracks	1380

Hard Disk	Cylinders	Tracks	Sectors	Bytes
1	230	1380	46,920	12,011,520
---	1	6	204	52,224
---	---	1	34	8,704
---	---	---	1	256

AC Power Requirements
- 50/60 Hz
- 100/115 VAC installations (90 to 127 V)
- 200/230 VAC installations (200 to 253 V)
- Fuse 2.5 Amps at 250 Volts (Internal)

Astec Power Supply (Primary Drive)
Operating Characteristics

		Min	Typ	Max	Units
Vin Range					
Input Select 115V		90	115	127	Vrms
Input Select 230V		200	230	253	Vrms
Line Frequency		47	50/60	63	Hz
Output Voltages	V1 +5V	4.95	5.1	5.25	Volts
	V3 +12V	11.4	12	12.6	Volts
	V4 -12V	-11.4	-12	-12.6	Volts
Output Current	V1 +5V	2.50		5.0	Amps
	V3 +12V	.75		2.0	Amps
	V4 -12V	.005		.10	Amps
Ripple Voltages	V1 +5V			50	mV
	V3 +12V			120	mV
	V4 -12V			120	mV
Efficiency		70			%
Hold Up Time					
Full Load, Low Line		10			mSec
Full Load, Nom Line		16			mSec
Over-Voltage Protection		5.80		6.80	Volts

Astec Power Supply (Secondary Drive)
Operating Characteristics

		Min	Typ	Max	Units
Vin Range					
Input Select 115V		95	115	135	Vrms
Input Select 230V		180	230	264	Vrms
Line Frequency		47	50/60	63	Hz
Output Voltages	+5V	4.75	5	5.25	Volts
	+12V	11.4	12	12.6	Volts
	-12V	-11	-12	-15	Volts
Output Current	+5V	.45		2.5	Amps
	+12V	.75		2.0	Amps
	-12V	.005		.10	Amps
Load Regulation (measured by varying load on considered output from typ to either min or max rated load)	+5V	5		5	%
	12V	-5		5	%
	-12V	-8.3		25	%
Ripple Voltages	+5			50	mV
	12V			150	mV
	-12V			150	mV
Efficiency		65			%
Over-Voltage Protection		5.80		6.80	Volts

Dimensions	
Height	5.5 in (140 mm)
Width	14. in (356 mm)
Length	15. in (381 mm)
Weight	
Primary	15.5 lbs (7.02 kg)
Secondary	12.5 lbs (5.68 kg)
Environment	
Ambient Temperature	50 to 95 degrees F. (10 to 35 degrees C.)
Relative Humidity	8% to 80%
Maximum Wet Bulb Temp.	78 F. (26 C.) non-condensing
Heat Dissipation	150 Watts (511 BTU/Hr)
Altitude	operating: 0 to 6000 feet (0 to 1829 meters) storage: Sea Level to 12000 feet (0 to 3656 meters)
Warm-Up Period	
Minimum On Power-Up	2 minutes
Minimum to Turn System On After Turning System Off	15 seconds
Hard Disk Drive	
Disk Organization	
Tracks per Unit	1380
Tracks per Platter	460
Sectors per Track	34
Bytes per Sector	256
Cylinders per Disk	230
Average Latency	8.34 msec
Rotational Speed	3600 rpm +/- 1%
Recording Density	9625
Flux Density	9625
Track Density	254
Storage Capacity (Hard Disk)	
Unformatted	
Bytes per Track	10400
Bytes per Surface	2.39 MEG
Bytes per Drive	14.35 MEG
Formatted	
Bytes per Drive	12 M (Primary) 12 M (Secondary)

3/ Interface Board Installation

Models II and 16

Connect (jumper) pins AK-AP, A-B, A-B, V-W on the Interface Board.

Insert the Interface Board.

Install the 50 pin connector in the back panel of the computer (below the disk expansion connector).

Connect the internal cable from the connector on the interface board to the 50 pin connector on the back panel of the computer..

Change R21 and boot ROM. Also modify CPU board.

Model 12

In order to install the interface board in the Model 12 the card cage must be installed first (see - Seven Slot Expansion Kit Instructions - 26-6017).

Connect (jumper) the following pins on the Interface Board.

Model 12   AC-AG, A-B, A-B, V-W.

Insert the Interface Board.

4/ Connections

Connecting Your Primary Drive

Be sure all power is OFF.

Note: The Master (Primary) unit does not come with Data Out connectors. These are supplied with each secondary unit and require installation.

Models II and 16

Connect one end of the hard disk expansion cable to the 50 pin connector on the back of the computer.

Connect the opposite end of the hard disk expansion cable to the COMPUTER IN connector, located on the rear panel of the primary drive.

Model 12

Locate the hard disk expansion cable. Connect one end of the cable to the Interface card connector of your Model 12 or 16. Be sure the cable exists the rear of the computer so that it won't bind.

Connect the opposite end of the hard disk expansion cable to the COMPUTER IN connector, located on the rear panel of the primary drive.

Connect the power cord to the primary drive. Plug the other end into an appropriate AC power source.

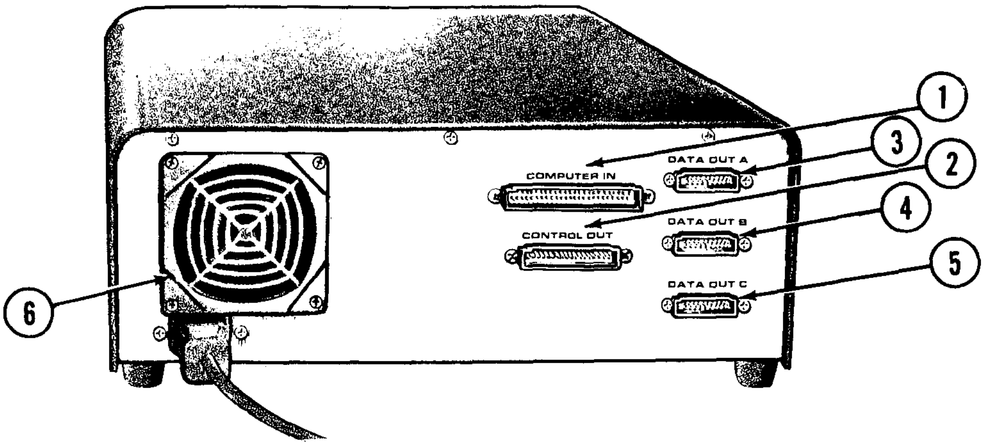


Figure 1. Back Panel of Hard Disk Drive

1. Computer In (50-pin) Connect the Hard Disk Expansion Cable from the Computer to this connector.

2. Control Out (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this connector. The other end connects to the first secondary drive.

3. Data Out A (20-pin) Connect one end of the Data Cable from the first secondary drive to this connector.

4. Data Out B (20-pin) Connect one end of the Data Cable from the second secondary drive to this connector.

5. Data Out C (20-pin) Connect one end of the ata Cable from the third secondary drive to this connector.

6. Filter

Connecting Secondary Drives

The secondary drives are connected to the computer via the primary disk drive. The drives must be stacked with the primary drive on top of the secondary drives.

Locate the secondary hard disk expansion cable. Connect one end to the Control In connector of the secondary drive and the other end to the Control Out connector of the previous drive in the chain. If you have only two hard disk drives, this connector connects to the primary drive.

If you have another secondary drive, connect the second secondary hard disk expansion cable to the Control Out connector and the other end to the Control In connector of the next drive in the chain.

Locate the data cable. Connect one end to the appropriate data connector (A for the first secondary drive, B for the second, and C for the third). Connect the other end to the Data In connector on the secondary drive.

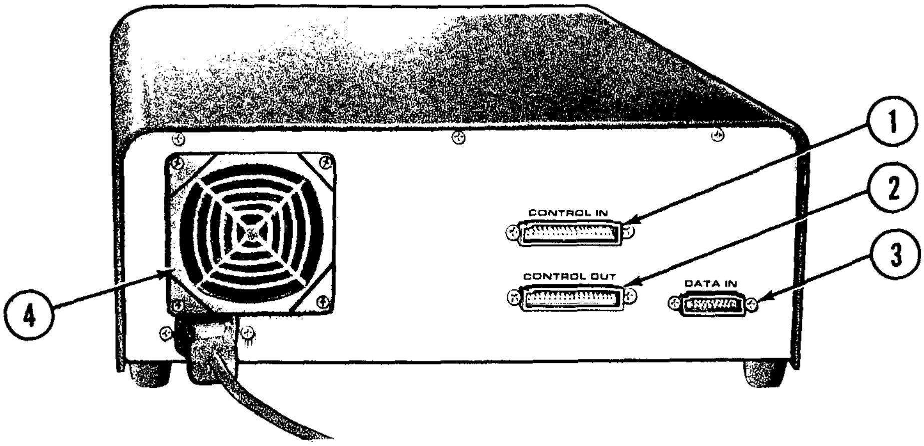


Figure 2. Back Panel of Secondary Hard Disk Drive

1. Control In (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this connector. The other end connects to the previous Hard Disk Drive.

2. Control Out (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this connector. The other end connects to the next secondary drive.

3. Data In (20-pin) Connect one end of the Data Cable from the the primary drive to this connector.

4. Filter

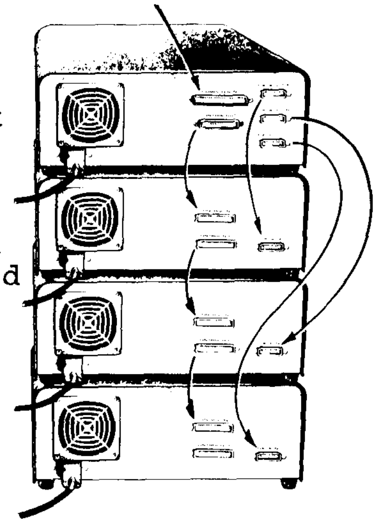


Figure 3. A Fully Configured Hard Disk System

5/Power-Up and Power-Down

System Power-Up

1. Make sure all power is OFF and all floppy diskette drives are empty.

2. Turn on all peripheral equipment (such as a printer or additional floppy diskette drives)

3. Turn on the primary hard drive by turning the POWER KEY clockwise. This also turns on all secondary drives. All secondary drives' power lights should come on.

4. Turn the computer ON.

5. Insert either the FORMAT diskette or the START-UP diskette in floppy Drive 0.

6. Press RESET. In a few seconds the screen shows a large TRSDOS II logo.

   If the TRSDOS II logo does not appear, repeat the above steps, making sure you inserted the diskette properly.

7. The screen then shows this prompt:

   TRSDOS II Ready

   Since you've not yet initialized your Hard Disk System, the computer is now operating as a Floppy Disk System, the only way it can operate until you initialize it.

   If you've initialized the Hard Disk System, you can remove the START-UP diskette. You only need it to start up or reset.

To operate the system for floppy disk only, hold down the <CLEAR> key and press the RESET button. (You must keep the <CLEAR> key down until TRSDOS II Ready appears.)

System Power-Down

1. The TRSDOS II Ready prompt should be the last line on your screen. If not, press <ENTER> or exit your program so that it appears.

2. Remove all floppy diskettes from their drives.

3. Turn off any peripheral equipment.

4. Turn off the hard disk drive by turning the power key on the primary drive counterclockwise. This turns off all the drives.

5. Turn off the computer.

6/ Replacement Procedures

Replacement procedures contained in this manual are limited to case disassembly, removal and replacement of subassemblies, and case assembly.

Before beginning repair, disconnect all external cables from the rear connector panel.

Disassembly

1. Remove the top row of screws (3) from the rear panel and lift off the case.

2. To remove the hard disk controller board, remove all cables from the board (data cables, hard disk expansion cable, controller connecting cables, power harness, and lamp controller harness).

NOTE: At the time of disassembly, be sure that the nylon washer on center stand-off is saved for reassembly.

3. To remove the hard disk power supply, remove the 4 screws which secure the power supply mount-and-shield to the bottom of the unit and lift off the cover. Loosen all cables. Disconnect the power harness from the drive unit. Remove the six screws which hold the power supply board.

Reassembly

1. Fasten the power supply in the bottom of the unit by using 4 #6 screws and 2 #10 screws. Reconnect the power cables.

2. Replace the power supply shield-and-mount and fasten it using 4 #6 screws. Reconnect the power harness on drive. Position the clear insulating sheet on the power supply mount-and-shield.

3. Be sure and replace nylon washer between the hard disk controller board and center stand-off. Fasten the board

using five #6 screws.

4. Reconnect all cables, the lamp driver harness, and the power harness. (Make sure that the lamp driver harness is toward the rear of the unit.) Be sure that the data cables are connected so that the cable comes from the left-hand side of the plug when looking from the front of the unit.

5. Replace the case top and 3 #6 screws in the rear panel.

7/ Maintenance

The only regular maintenance the 12-Meg Disk Drive requires is a periodic cleaning of the filter on the back of the unit. Clean this filter whenever it becomes filled with dust and particles.

To clean the filter, carefully remove the outer grill -- DO NOT REMOVE THE SCREWS. Then remove the filter and rinse with tap water. When the filter is completely dry, put it back in the drive.

8/ Theory of Operation

Hard Disk Controller Board

General

The hard disk controller board is a discrete implementation of all functions required to control the 5.25 inch disk drive via a standard data and control bus. The controller is fabricated using a mix of high-speed bipolar and MNOS devices contained on a single two-sided PC board. The design of the circuitry makes use of a high-speed microcontroller, the 8X300, newly developed NMOS support devices, Schottky and low power Schottky devices. All I/O connections are made using standard ribbon cable connectors. Standard pin-out configurations for disk interface connectors permit direct pin-for-pin connections to the drives. All host to disk data transfers are buffered by onboard RAM to achieve totally asynchronous transfers to and from the disk by the host.

The disk controller is built around five basic sections:

Processor Functions

All functions of the controller are ultimately disciplined by the onboard processor. Due to the high data rates associated with hard disk drives, a processor capable of extremely fast execution speed is required for processing of data and controlling machine functions within the circuitry. The processor used is the 8X300, a bipolar micro-controller particularly well-suited for handling data efficiently at high rates.

The 8X300 operates at a basic clock rate of 8MHz and performs all operations within two clock cycles giving it a speed of 4 MIPSS (Million Instructions Per Second) or one instruction executed every 250 nanoseconds. The architecture of the processor is different from most popular microprocessors in that no common data or address bus is provided to be shared by RAM, ROM, or peripheral devices.

Instructions are fetched from ROM via a dedicated instruction address and data bus. The Instruction Address bus (IA0 - IA13) is capable of directly accessing 8K words of program storage, however, the controller uses only the first ten address lines, IA0 through IA9, limiting onboard program storage to 1K words.

Program data is input to the 8X300 (U42) on the Instruction Data bus (IAO - IA130) which is capable of directly accessing 8K words of program storage; however, the controller uses only the first ten address lines, IAO through IA9, limiting onboard program storage to 1K words.

Fast IO Select

An extension byte has been added onto the instruction data memory to provide port access decoding on an instruction-by-instruction basis. This "Fast IO Select" byte is not processed by the 8X300, but it is decoded by auxiliary hardware (U39, U44, U45) to provide eight read strobes and eight write strobes which route data to the various devices distributed along the interface vector bus.

The Fast IO byte is latched into a 6-bit latch (U39) trailing edge of MCLK to ensure that the data remains stable during the entire instruction. This data selects a read strobe and eight write strobes which route data to the various devices distributed along the interface vector bus.

The Fast IO byte is latched into a 6-bit latch (U39) trailing edge of MCLK to ensure that the data remains stable during the entire instructions. This data selects a read strobe and a write strobe through two 1-of-8 decoders (U44 and U45) which are alternately enabled by the WC* control strobe produced by the 8X300. THe read strobe decoder (U44) is always disqualified at the end of instructions by MCLK' (MCLK prime), a delayed copy of MCLK, to provide edges on read strobes during sequential read operations from various ports. This delay compensates for timing races through the Fast IO latch (U39) and the control signals.

Because each decoder has a unique input, it is possible to select any read port with any write port during each instruction. Data is transferred between the processor and its ports on a separate 8-bit bus called the IO bus. This bus is active low. It must be noted that this bus is in no way related to the instruction data bus and should be thought of as simply an 8-bit bidirectional IO bus of the 8X300. In fact, it has been renamed as IO0 - IO7 to reflect this distinction.

Internal Bus Control

Several bus control signals are produced by the 8X300 to identify and strobe the data on the IO bus. Write Control

voltage reference is provided to produce bias to an external pass transistor (Q2) which drops Vcc to the 8X300 to approximately +3 volts. All signals into and out of the 8X300 are internally level shifted to be TTL compatible.

Read and Write Ports

Throughout the circuit, output ports are formed by "D" type latches using write strobes (WR0 -WR7) to latch data into the ports. Reading of ports is universally accomplished by using read strobes (RD0, RD2, RD4 - RD6) that enable selected tri-state output devices on the I/O bus. Additionally, two read strobes are used to clock the host DRQ* and INTRQ* latches (U5) and one read strobe is left unused as a "dummy" port for glitch-free operation of the Fast IO port decoders.

Read/Write Memory

Since the 8X300 does not permit data to be saved or retrieved from dedicated program storage, RAM must be installed on the IO bus. RAM must be accessed just like other port accesses via the IO bus by IO instructions. To provide for addressing the RAM, three latch/counters (U26, U27, U28) are connected to the IO bus to receive and store addresses required to access the RAM (U17,U18).

RAM Addressing

The RAM address bus (RA0 - RA9) uniquely addresses one of 1024 memory locations. As each counter chip reaches a count of 0, it will set a borrow condition to the next higher counter which will be decremented at the end of the next access to RAM. When all bits of the address have been reset, the ROVF* bit on the last counter (U26) will be reset, providing overflow status which can be read by the processor on (U26). By setting various beginning address values, ROVF* can be used to mark the end of any RAM access loop from 1 to 1024 bytes in length. The controller board uses this function to set sector buffer lengths of 128, 256, or 512 bytes.

Sector Buffering

All data read from or written to the disk is passed through the RAM to provide buffering required for asynchronous data transfer between the host and disk. The counters are post-decremented, which means that the effective addresses are stable to the RAM by at least the instruction prior to

separation. Here, some background information may be helpful:

> In order to provide maximum data recording density and therefore maximum storage efficiency, data is recorded on the disk using a Modified Frequency Modulation (MFM) technique. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. This reduces the total number of bits required to record a given amount of information on the disk. This results in an effective doubling of the amount of the data capacity, hence the term "double density."

Because clock bits are not recorded with every data bit cell, circuitry that can remain in sync with data during the absence of clock bits is required. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bits when they are present. This is accomplished by using a phase-locked oscillator employing an error amplifier/filter to sync onto and hold a specific phase relationship at the data and clock bits in the data stream. The synthesized clock called RCLK can then be used to separate data bits from clock bits and to shift the resultant serial data into registers for parallelization into bytes.

Incoming Data Selection

Serial data is input from up to four radially connected drives via a quad RS-422 differential receiver (U54). The receiver converts differential input data to TTL levels for use by the controller. The data from the selected drive is then routed to gate (U53). At this point, data and clocks are still combined and appear as 50 nanoseconds (nominal) active high pulses spaced at intervals of one, one and a half, or two times the RCLK period. This data is presented to the input of another AND/OR/INVERT gate (U4) which will gate either MFM data or a reference clock into the first stage of the VCO error amplifier circuitry.

Reference Clock

The reference clock is derived from the write clock crystal oscillator (Q1, U10, and associated circuitry). This oscillator uses a fundamental cut crystal to oscillate at four times the RCLK frequency. The 4X output is then divided by U10 to produce both a 2X clock (2XDR*), which is used as a reference, and a 1X clock (WCLK) which is used to produce

MFM write data for the disk. The crystal (Y1) frequency is 20.000 MHz for compatible drives.

Clock Gating

The gating of the reference and MFM data into the data separator is dependent upon the condition of the Read Gate signal (RGATE) and the spacing of the data on the serial stream after RGATE is brought true. Due to the techniques which are employed to separate data from clocks, it is necessary to run the VC0 at a rate twice the data clock (RCLK) rate. The VC0 is therefore set to an open-loop frequency of 2 times RCLK. Any variations in this rate due to variations in disk rotational speed must be compensated for by the VC0, but instantaneous shifts in data due to the effects of adjacent bit cells on the disk and minor noise must be ignored. Also, the response of the VC0 must be adjusted to effectively ride over missing clock bits which occur as a result of MFM recoding technique. The resultant compromise between response and reject requirements of the VC0 cause the VC0 to have a tendency to become locked onto harmonics of the data rate rather easily. This is likely to occur if the VC0 is connected to a data stream over a field of data which has data bits spaced at one and a half or two times the actual RCLK time intervals.

To provide protection against this undesirable condition, the VC0 is always held locked onto a stable clock running at two times the RCLK frequency whenever the controller is not actually reading data. Furthermore, great care is taken to switch in read data to the VC0 error detector only when it is known that the data stream frequency is equal to the RCLK frequency. This can occur only when the data is a solid stream of all ones or all zeros.

High Frequency Detector

The switching function is initiated immediately after RGATE goes true and will only switch read data into the VCO after 16 consecutive ones or zeros (high frequency) are detected by a one-shot (U1) and counter (U2) connected directly to the raw MFM data. The one-shot is adjusted for a pulse width of one and one-fourth times the RCLK period. This is 250 nanoseconds, +/- 10 ns. These adjustments of the the DRUN one-shot (U1) provide tolerances of up to one-fourth the RCLK period in jitter on the MFM data bits while still being able to distinguish MFM zeros or ones from other data patterns.

Each clock or data bit on the serial stream triggers the one-shot. If the time between successive triggers is less than the one-shot time constant, the one-shot remains retriggered. As the one-shot is triggered by data stream bits, so is the up/down counter (U2) whose count mode is controlled by the state of the one-shot outputs. While the one-shot is being retriggered, the counter counts up. When any data bit fails to reach the one-shot before its time constant is over, the one-shot resets and in turn clears the counter. Only when 16 successive retriggers occur, can the counter reach its terminal count. At this time, the counter overflow goes true and sets the DRUN* latch output (U3, pin 6) low which switches read data in and reference clock out. An AND-OR-INVERT gate (U4) performs the switching. DRUN* is read through (U74) by the 8X300 to determine the condition of the MFM data stream.

VCO

The Hard Disk controller uses a single chip VCO (U32) which simplifies circuitry and adjustments. The operating point of the VCO is initially set by adjusting the variable capacitor (C33) for a 10 MHZ output at TP9 and the frequency control voltage input (TP8) to 2.5 V +/- .5 V. It should be noted here that both of these adjustments are done using the same trim cap (C33).

The output of the error amplifier and filter is fed to the VCO and represents how far the VCO frequency is from that of the incoming signal. The error signal, which is proportional to the difference, allows the VCO to shift from center frequency and become the same as the frequency of the frequency of the input signal. When the loop is in lock, the difference frequency component will be DC and is passed by the low pass filter.

Frequency control is actually a matter of frequency range. The difference component may fall outside of the band edge of the low-pass filter and be removed along with the sum frequency component. If this is the case, then no information is transmitted around the loop and the VCO remains at its initial free running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the filter. Now part of this difference component is passed which tends to drive the VCO to the frequency of the difference component more and allows more of it to be passed through the filter. This is a positive feedback, which causes the VCO to snap into "lock" with the input signal.

The term "capture range" can be described as the frequency range centered about the VCO free running frequency over which the loop can acquire lock with the incoming data signal.

The free running frequency of the VCO is always twice that of the RCLK rate. In fact, RCLK is produced by the VCO through a divide-by-two counter (U14).

Power for the VCO's internal oscillator as well as for the error amplification filter is supplied from a 78M05 +5 volt regulator. This insures good noise separation for these stages from the power supply.

Error Amplifier

Control of the VCO is accomplished by the error amplifier, filter, and Data Separator chip. The error amplifier is a balanced current mirror whose output sources or sinks current to the filter stage. Whenever the VCO is running too slow, the error amplifier receives pulses from data bits before pulses from the VCO clock. This causes the error amplifier to produce pump-up pulses to the filter. The filter integrates these UP pulses and raises the overall voltage of the voltage control input (TP8) to the VCO. When the VCO is running too fast, the error amplifier produces pump-down pulses to the filter. There will always be some error present because without pulses of UP and DN the filter would float causing the VCO to drift off center frequency.

Phase Detector

The circuitry which feeds the error amplifier is called the phase detector. This consists of several "D" latches (U20, U21) and a delay line (U31). The function of this circuit is to provide time windows during which the leading edges of the incoming MFM data can be compared to the leading edges of the VCO clock. These windows are approximately 50 nanoseconds in length and are initiated by the leading edge of any data bit as it enters the detector. The windows are terminated by the same data bit, edge delayed by a net of 50 nanoseconds (60 nanoseconds in the delay line minus approximately 10 nanoseconds in propagation delays.) When both the delayed data bit and the nearest VCO clock edge arrive at the detector, the detector is reset until the next data bit arrives on the MFM data stream. The delayed data bit sets its half of the detector latches to produce the VP pulses. The VCO clock edge sets its half of the detector to produce the DN pulse.

Window Extension

Once the VCO has been locked onto the phase of the incoming data, the actual separation of data and clocks can occur. This is accomplished by using a technique called window extension. This technique causes data bits to first have their leading edges shifted into the center of the RCLK half cycles then to have them latched or extended until the next rising edge of the RCLK. The shift is accomplished by tapping the data of the Sample on Phase Detector delay line at the 60 nanosecond tap, and inverting the VCO clock to the RCLK divider (U14). The delayed data clocks a pair of latches (U12 and U13). The "data" latch has its "D" input and CLEAR connected to RCLK* and the "clock" latch has its "D" input and CLEAR connected to RCLK*.

If an MFM data bit enters the latches while RCLK is high, it will be extended as a data bit. If RCLK* is high, it will be extended as a clock bit. Due to this extension technique, bits can jitter approximately one-fourth the RCLK period without being lost. The output of each latch is then further extended by being fed directly into the second half of the latches and clocked on alternate edges of RCLK. The final outputs of the data extension/separation stage are two separate signals; one signal consists solely of NRZ (non-return to zero) data and the other of NRZ (non-return to zero) clocks. The NRZ data and clocks are finally in a form suitable for processing by subsequent circuitry on the Controller board.

Clock Detection

Due to the nature of MFM data encoding, it is impossible to know exactly if MFM bits are data or clocks. This ambiguity results in having to create circuitry to assume that bits on RCLK* are actually data bits until the VCO is locked on and a unique data/clock pattern is detected. This is accomplished by holding the VCO to RCLK divider (U14) reset until it is fairly certain that bits on the data stream are actually clocks belonging to a field of zero data.

Once this assessment has been made, the processor releases the AM detector (U11) by raising the SRCH signal. This signal releases a latch (U20) which will remove DHOLD from the RCLK divider (U14) on the next rising edge of a MFM data bit so that CLOCKS will be on the RCLK* phase and DATA will be on the RCLK phase. The processor makes its assessment of the state of the data stream solely on the occurrence of a significant run of zeros which is detected by the one-shot (U1) in the DRUN circuit. Once released, the phase of RCLK vs. data and clocks will remain stable throughout the read of an ID field or data field. Whenever SRCH is dropped, the VCO to RCLK divider is once again reset and no RCLKS are produced.

Data Conversion and Checking

MFM data which has been separated to form NRZ data and clocks is processed through specialized circuitry to prepare it for parallel processing by the 8X300. This processing consists of three functional circuits.

1. AM detection (U11)
2. Serial-to-Parallel conversion (U9)
3. CRC checking circuit (U6)

Each function will be discussed separately but bear in mind that many interdependencies exist.

AM Detection

As previously stated, it is impossible to know whether serial data bits are actually data or clock bits by just looking at the data stream. Furthermore, it is equally impossible to determine byte boundaries. The problem is solved by a uniquely recorded data/clock pattern called an Address Mark (AM). The AM consists of a data pattern of HEX 'A1' with a missing clock pattern of HEX '0A'. Normally a data byte of of HEX 'A1' requires a clocking pattern of HEX '0E'. In fact, due to the rules of MFM data encoding, an alternating clock pattern such as HEX 'A' or HEX '5' cannot exist legally.

The AM is used to uniquely identify the start of a field of information (data or ID field) within each sector. A long run of zero data always precedes each AM on the disk. Zeros have a clock bit for every RCLK. When attempting to read information from the disk, the Controller first acquires phase lock over a field of zeros. When this acquisition is achieved, the processor releases the AM detector (U11) by raising the Search control line (SRCH) on the MAC CNTRL port (U29).

Due to the circuitry associated with the VCO to RCLK divider, the RDAT* output of the data separator (U13 - 8) will be high and the CLKS* output (U12 - 8) will be low. RCLK* will be the shifting clock for RDAT* and RCLK will be the shifting clock for CLKS*. These four signals are routed into the AM detector. Inside the AM detector, RDAT* is shifted into an 8-bit synchronous serial shift register and clocked on the falling edge of RCLK*. CLKS* is shifted into a similar shift register on the falling edge of RCLK. The output stage of the RDAT* register is dumped into an 'Al' comparator and the output stage of the CLKS* register is dumped into a '0A' comparator. AM detection occurs when both detectors are true, thereby setting the AMDET* latch. At the instant AM occurs, the exact relationship between data and clocks is known. It is also known that data is being clocked by RCLK* so CLKS* can actually be discarded; their purpose was in detecting AM. The AMDET* signal is used as a synchronization signal to start subsequent conversion circuitry. The AMDET* signal remains true until the processor again de-asserts the Search control line.

Serial to Parallel Conversion

After an AM has been detected, the serial-to-parallel convertor (U9) takes over. NRZ data and RCLK are used to shift data bits into an 8-bit serial-to-parallel shift register. As each bit is shifted, a divide-by-8 counter circuit is incremented. After every eighth bit of data is shifted, the counter produces an overflow pulse marking byte boundaries in the serial data stream. The overflow bit from the counter resets the counter, clocks the data from the shift register into an 8-bit parallel latch, and sets a tri-state flag register called BDONE. The flag can be read by the processor to see if any converted data is ready to be read from the latches.

When the processor sees BDONE in the true state, it services the device by gating data onto the IO bus using read strobe 4 (RD4*) in conjunction with a tri-state buffer (U8). The act of reading the latches also clears off the pending BDONE flag. As successive bytes are processed, the BDONE is serviced by the processor as data becomes available.

Outputs from the serial-to-parallel device also include SHFTCLK* and DOUT. SHFTCLK* is actually RCLK* propagated through the device. DOUT is the Q output of the last stage of the shift register string. DOUT and SHFTCLK* are routed to the CRC generator checker device and also are tri-stated along with BDONE. These signals are active only when WRITE* is high which indicates a read mode of operation.

CRC Checking Circuit

Data recorded on magnetic media is prone to several types of errors which could render data unusable if some form of error detection were not employed. Therefore, a cyclic redundancy check (CRC) is performed on all data transfers from the disk. The CRC is an error detection code consisting of 16 additional bits which are appended to every ID field and data field on the disk. These bits are produced by dividing the data stream serially with a large polynomial. This division produces a unique 16-bit value for any information passed through the CRC generator.

As data is being read from the disk, the CRC generator (U6) re-computes the original CRC bits. The value in the CRC generator must always be zero after the last two bytes (which contain the orginal recorded CRC) are read. When this happens, the data was correctly read and the controller will not flag an error. If, however, the CRC generator is not zeroed after it has checked all bytes of the recorded data, the controller will flag the data as erroneous and enter into a re-try condition. If the controller cannot get correct data after attempting to read it 16 times, the read will be aborted and the host informed that the data in the buffer is questionable.

The Controller board uses the same device to generate and check CRC's for data being written to or read from the disk. The polynomial used is:

$$X^{16} + X^{12} + X^{5} + 1$$ (commonly called the CRC-CCITT polynomial)

The processor polls the condition of the DRUN circuitry during read operations. When DRUN is true, it begins to search for an address mark. Once the AM is located, the processor will start to read parallel data which has been converted from NRZ data by the serial-to-parallel device. The processor will terminate this activity when it has received the information it is looking for or if an error is detected.

While the processor is reading the parallel data, the CRC generator is reconstructing the CRC check value. The CRC generator is initialized by the processor setting CRCIZ* low for at least 250 nanoseconds during the search for the AM. CRCIZ* is originated on the MAC CNTRL port (U29). Upon receiving the CRCIZ* signal, the CRC generator/checker will preset all 16 of its internal polynomial division shift registers to logic ones and arm an internal latch which will enable the checking function on the leading edge of the first non-zero data to enter the device. It should be remembered that prior to an AM there is always a field of zeros (all data bits low) so the first non-zero data bit into the device will always be the most significant bit of the AM (HEX A1).

The CRC device, when enabled by the first non-zero data bit, will shift succeeding data bits into a feedback shift register string with Exclusive or gates tied to the feedback nodes on the first, fifth, twelfth, and sixteenth registers. As each RCLK occurs, the registers will divide the incoming data and a unique pattern of ones and zeros will appear across the registers.

When the last bit of an ID or data field is processed, the pattern in the registers should be equivalent to the 16 bits appended to the fields during original recording. The appended bits are also entered into the CRC device. If all of the bits in the appended field are identical to the bits in the registers, then the Exclusive-or-Gates in the register string will have flipped all of the ones to zeros and the CRC will have been satisfied.

The output of each register stage is tied to a 16-bit comparator which goes true when all of its inputs are zeros. The output of the comparator is retimed to remove any decoding slivers and is output as CRCOK. The processor can read CRCOK through U61 to see if a CRC error has occurred.

After the CRC bits are processed, the data stream will contain at least one more byte of zeros. It is the nature of the CRC polynomial that if no bits are set to ones in the registers and if a constant input of zeros is shifted into the registers, no bits will be flipped. This provides a convenient latching function for the CRCOK flag which will remain true for at least one byte after the last CRC check byte, giving the processor time to read the flag.

The data, clock, and BDONE are supplied to the CRC device on a 3-bit mini bus. During read operations, the serial-to-parallel device (U9) will be sourcing these lines since the WRITE control line from MAC CNTRL (U29) is low and this enables tri-state drivers on these lines. The

Parallel-to-Serial device (U7) will have its tri-state drivers disabled.

Serial Data Generation

The Controller records data on the disk in MFM format. In order to produce the proper data format, the Controller uses several specialized devices to process the parallel data supplied by the host into a serial MFM data stream. The data supplied by the host is temporarily stored in the buffer RAM until the correct sector is located for the data to be written.

The process of writing is essentially the opposite of reading except that the data separator circuitry is not required and the generation of the MFM data stream is produced by synchronous clocking techniques.

The functional sections of the serial data generation section are listed below:

1. Parallel-to-Serial conversion (U7)
2. CRC generation (U6)
3. MFM and precompensation (U5)

Parallel to Serial Conversion

Parallel data is converted into a serial NRZ data stream by the parallel-to-serial device (U7). The processor enables this conversion by lowering the WRITE* signal on MAC CNTRL (U29). WRITE* causes the tri-state buffers present on the parallel-to-serial device to become active, supplying the CRC device with data, clocks, and BDONE strobes.

The processor presents parallel data on the IO bus along with the WR4* write strobe which latches the data into the parallel port on the BDONE. Inside the parallel-to-serial device, the parallel latches are loaded into a serial shift register on every eighth WCLK transition. As the data is transferred to the shift registers, the BDONE status flag is set. The processor reads this flag through U61 to determine when to write the next parallel byte to the device. The timing of the parallel accesses is at a rate one-eighth that the bit rate of the NRZ data stream.

The output of the last register in the shift string is brought out of the device as a NRZ serial data stream. The shifting clock is also brought out as SHFTCLK to be used as the clock for the CRC device.

Whenever it is desired to write a repetitive string of identical data bytes, the processor can simply ignore the BDONE flag and permit the device to reload the data from its latches over and over again for as long as required to generate the field. This feature of the device is used in writing certain fields used in formatting.

CRC Generation

The CRC generator/checker (U6) is used to generate the CRC bits and to append them to the end of the data being written to the disk. This is the complementary function to that performed during reads. The operation of the polynomial generator is identical to read operations except that at the end of the data field, the processor sets a signal which causes the device to output the computed CRC after the data instead of reading the CRC and checking it.

The initial state of the shift registers within the device is forced to all ones by the processor pulsing CRCIZ* for approximately 250 nanoseconds while the parallel-to-serial device is outputting all zeros on the NRZ data line. At that time, a latch is set which holds the registers at ones until the first non-zero bit enters the device. The first non-zero bit will be the MSB of the AM (HEX A1) of the data field to be written. When the processor decides that enough zeros have been written to satisfy the sync field requirements, it will store a HEX A1 in the parallel-to-serial device. At the proper time (in sync with BDONE) the parallel-to-serial device will begin to send the MSB of the AM to the CRC device. This will start the CRC polynomial generator and the CRC will be computed.

As the processor writes the last byte of data to the parallel-to-serial device, it will drop the 1BLA* (1 Byte Look Ahead) signal on MAC CNTRL port (U29). This signal will cause the CRC generator (U6) to begin dumping the computed CRC onto the NRZ data stream at the conclusion of the last data byte (synchronized with the BDONE signal). In this fashion, the device is able to append the proper CRC information to the end of a field of data. 1BLA* is maintained at a low state for the duration of the unloading process which lasts for 16 bit times.

During the unloading process, the CRC registers back-fill with zeros. This feature is handy because by leaving 1BLA* low; for additional time, zeros will always be written after the CRC which is a requirement for the proper operation of the CRC device during read operations. The NRZ data with CRC appended is then sent to the MFM generator device (U5).

MFM Generation

The conversion from NRZ write data to MFM write data takes place in the MFM/Precompensation device (U5). This device accepts NRZ data and a complimentary WCLK and produces MFM data and clocks by sending the data through circuitry which decides when and where to write clocks on the data stream under the MFM encoding rules. The proper encoding of the data into MFM requires the device to apply three rules to the data.

1. If the current data cell contains a data bit, no clock bit will be generated.

2. If the previous data cell contained a data bit, no clock bit will be generated.

3. If the previous data cell and the present data cell are vacant, a clock bit will be produced in the current clock cell.

The terms "data cell" and "clock cell" are defined by the state of WCLK. While WCLK is low, it is a data cell and while high, it is a clock cell. It can be seen then that both clock and data cells are one-half the period of WCLK or 100 nanoseconds. Also note that by the rules started above, a clock and data bit can never occur within the same WCLK period and legal spacings for bits can be one, one and a half; or two times the WCLK period only. The rules are implemented within the device by shift registers that hold the next two, last, and present data bits and combinational logic. The state of WCLK is considered and the appropriate bit cells are filled and combined on the MFMW output line of the device. This line is subject to decoding slivers, so it is run through a re-timing latch (U16) to clean it up.

Write Precompensation

The MFM data stream is now totally compatible with the recording rules and may be sent to suitable line drivers for transmission to the drive except for one modification. Due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem in magnetic recording known as dynamic bit shift.

Dynamic bit shift occurs as the result of one bit on the disk (a flux reversal) influencing an adjacent bit. The effect is to shift the leading edge of both bits closer together or further apart than recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error. In any event, there is a method called write precompensation which can be applied to reduce the effect of this shift on the data.

Write Precompensation is a way of predicting which direction a particular bit will be shifted and intentionally writing that bit out of position in the opposite direction to the expected shift. This is done by examining the next two data bits, the last bits, and the present bits to be written and producing three signals depending on what these bits are. The three signals are EARLY, LATE, and NOM. They are used in conjunction with a delay line to cause the leading edge of a data/clock bit to be written early, late, or on time. As with MFMW, these signals are subject to decoding slivers and must be retimed by U16.

The processor can enable or disable the generation of these signals by controlling the RWC (Reduce Write Current) line from U52. When RWC is high, precompensation is in effect. When RWC is low, no precompensation is generated and the NOM output of the device is held true.

The delay line, U31, actually performs the precompensation with the help of an AND-OR-INVERT gate (U37). The MFMW pulses are applied to the input of the delay line and, depending on which of the three precompensation signals is present, the U37 selects a different tap on the delay line. Nominal data is actually tapped from the second tap, early data from the first, and late data from the third. From U37, the MFMW data is sent to the input of a quad driver (U35 or U36) where it is converted to a differential form and then sent to the disk drive. The AND-OR-INVERT gate (U37) has one other function. If the controller is not writing, the WGI (Write Gate Internal) signal will be low. This is inverted by U19 and applied to the fourth section of U37. This resulting high input effectively inhibits the gate from accepting MFMW data.

Host Interface

The interface bus to the controller is pin-for-pin compatible with the standard I/O port. This includes an 8-bit bidirectional data bus (U70) and 8 address lines (U71). For systems using interrupts and/or DMA, the controller also provides Interrupt Request (HDBINTRQ*) and Data Request (HDBDRQ*).

Accessing the controller is like other I/O devices. Address decoding is done on the controller board by U69. This decode can be jumpered to recognize four different address ranges. Standard setting is jumpered from 17 to 19, which utilizes port locations C0 to CF HEX. Further decoding to allow access of specific ports is done by U66, U67, and U68. Data bus direction is determined by U56, using standard bus as well as decoded signals.

Wait Enable

The generation of the WAIT* signal is controlled by a bit in the MAC latch (U29) called Wait Enable (WAEN*). If the controller is ready to accept random access to its task file, WAEN* will be asserted. After WAEN* is clocked through a latch (U43) to insure WAIT* is not asserted during a bus access in progress, DCRCS* (BIC or BOC in some applications) causes WAIT* to be asserted to the bus.

The WAIT* line is released on the trailing edge of any Read or Write Strobe to the communications latch, U60. This release is caused by the logical OR of RDG* and WRG* on U38 which presets the wait latch, U43, to a non-wait request condition.

Interrupts and DRQ's

The controller produces INTRQ* to signal the end of all disk operations and DRQ's to signal data ready to DMA controllers. INTRQ* and DRQ* originate on the MFM generator (U5) as an auxiliary function of that chip. The INTRQ* signal is set using INTCLK and the the DRQ signal is set using DRQCLK, both of which are produced by U44. Interrupts are cleared by CSAC'* (a 200 nanosecond version of the CSAC signal) and A0, A1 whenever the host reads the status register, issues a command or accesses the sector number register. Data requests (DRQ's) are cleared when the host accesses the data or cylinder low registers DRQ's will be reissued for each byte to be transferred. During power on or Master Resets (MR*), INTRQ* is set and DRQ is reset.

Interface Board

Features

- Standard Model II Bus Interface
- On Board CTC For Interrupt Control
- DMA Operation Capability
- Internal 16K Dynamic RAM
- Handles Up To 4 Disk Drives

Signal Interfacing to Model II Bus

Data is passed betweeen the interface board and the Model II type system bus via one 8303 transceiver, U40. Address and control signals are taken off the system bus and buffered by two LS240 inverting drivers. U42 carries the address lines and U43 carries the control signals. Also two signals are driven onto the system bus by U39, using two of its four open collector output nand gates. These two Model II signals are WAIT* and XFERRQ*. All of the above signals lead to J1, an 80 pin edge connector which plugs into a standard Model II type mother board.

Signal Interfacing to Hard Disk Controller Bus

Data is transfered to the HDC bus in the same manner as to the Model II bus using one 8304 non-inverting transceiver, U13. Address lines A0 through A7 are driven onto the HDC bus by U14, an LS244 non-inverting buffer. Another LS244 driver, U15, is used to supply the HDC bus with all necessary control signals as well as suppling the following signals to the interface board from the HDC; HDBWAIT*, HDBINTRQ*, and HDBSEL*. HDBSEL* is used as a direction switch for the interface to HDC data bus.

All communication between the interface board and the external HDC is done through J2, a 50 position right angle pin header. A ribbon cable leads from J2 on the board to a 50 pin I/O header mounted on the back panel just below the connector for the floppy disk expansion bay.

Port Decoding Logic

The hard disk has 16 port mapped addresses for control and ID registers. A jumper setting (A to B for ports C0-CF) is used to determine the addresses to be decoded as an access to the HDC. The hard disk for the Model II is mapped from C0 to CF HEX. Other port ranges may be selected via this jumper scheme. However, existing software is intended only for use in the C0-CF ports.

U28, a 74S138, is used to decode the upper nibble of the port byte address. There are four outputs available from U28, each corresponding to a group of 16 port addresses. Selection of the port range is done by means of a single jumper as mentioned above. The following are jumper options for these port range options: A-B (C0-CF HEX); A-C (70-7F HEX); A-D (60-6F HEX); A-E (50-5F HEX). The selected output signal at A is the enable for one-half of U30, a 74S139 two into four decoder. U30 uses address lines A2 and A3 to give the outputs SELDCR* (select device control register), CTCCE* (CTC enable), or SELDIR* (select device ID regester).

CTCCE* is gated with DEVEN to form the signal CTCCS* which when active low indicates an access of the on-board CTC.

SELDIR* is also gated with WRID* by U23 and tied to the enable of one-half of U30. Only one of the four outputs is used and that is called WRDIR1* which when active low indicates a write operation to port C1. This signal latches the data bus onto the outputs of U35. This 74LS273 latch is used to provide the following signals to the interface board: DEVEN, INTRQEI, DMAEI, and SFTINT.

U38, a 74S64, is a multiple input AND-OR-INVERT gate. The output of this after being inverted again by one-sixth of U31 is used to enable the bus transceivers to either write data to or read data from the Model II bus. This signal is called M2DEN and when active (high) data is written to the system bus from the interface board.

CTC

The Z80 CTC (U22) on the interface board provides the Model II with an interrupt vector for up to four interrupting conditions from the hard disk contoller. CTC channels 0 to 3 are port mapped from locations C4 to C7 respectively (when using port ranges C0-CF). The CTC uses the standard Z-80 system interrupt protocol where interrupt priorty is determined by a peripheral device's location in the daisy chain. Because of this there cannot be an open card slot on the Model II mother board between the CPU board and the interface board.

16K Dynamic RAM

The 16K bank of memory on the interface board is set up the same as the memory on the Model II memory board. This RAM is jumpered to replace locations 8000H to BFFFH, bank F of the standard memory board's RAM.

For a detailed description of the memory address and data decoding see the Model II Technical Reference Handbook (#26-4921).

9/ Troubleshooting the Power Supply -Primary Drive
Section 1

Equipment for Test Set-Up

1. Isolation Transformer (minimum of 500 VA rating)-

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0-140 Variable Transformer (Variac)-
   Used to vary input voltage. Recommend 10 Amp, 1.4 KVA rating minimum.

3. Voltmeter-
   Needed to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

4. Oscilloscope-
   Need X10 probe.

5. Load Board with Connectors-
   See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

6. Ohmmeter

Set-Up Procedure

Set-up as shown in Figure 4. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 50mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of Section III for test points within power supply.

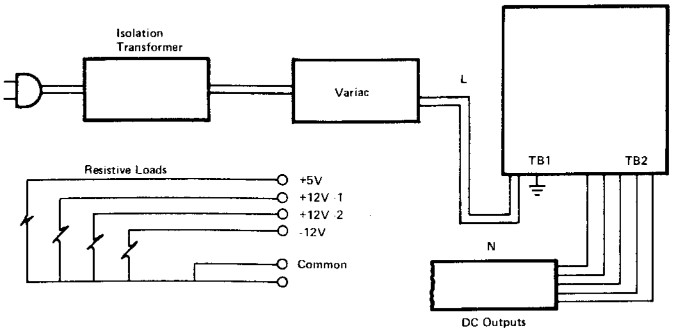


Figure 4. Test Set-Up

Section II

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

OUTPUT	MIN LOAD	LOAD RESISTANCE	SAFE LOAD POWER	MAX LOAD	LOAD RESISTANCE	LOAD LOAD POWER
+ 5V	1.35A	3.7 ohms	12.5 watts	4.0A	1.25 ohms	50 watts
+12V-1	0.40A	30 ohms	10 watts	2.1A	5.7 ohms	50 watts
- 12V-2	0.60A	20 ohms	15 watts	1.5A	8 ohms	35 watts
- 12V	0.0 A	1K ohms	1 watt	0.1A	120 ohms	3 watts

Table 1. Load Board Values

Start-Up

Load power supply with minimum load as specified om Table 1. Bring power up slowly with Variable Transformer while monitoring +5 output with scope and DVM. Supply should start with approximately 40-60 VAC applied and should regulate when 90 VAC is applied. If output has reached +5 volts, do a performance test as shown in Section IV. If there is no output, refer to Section III.

Load power supply with minimum load as specified in Table 1. Bring power up slowly with Variable Transformer while monitoring +5 output with scope and DVM. Supply should start with approximately 40-60 VAC applied and should regulate when 90 VAC is applied. If output has reached +5 volts, do a performance test as shown in Section IV. If there is no output, refer to Section III.

Section III

NO OUTPUT

General

When the AC input is applied to the L & N connections and the power does not produce an output, and power switch is on, one or more components have failed. A no output fault condition is most likely caused by a shorted/open component on the primary side but may also be caused by a short on the secondary. To determine the cause follow the steps below.

A. Check Fuse
If fuse is blown, replace it, but do not apply power until the cause of failure is found.

B. Preliminary Check on Major Primary Components
Check diode bridge (DB1), power transistor (Q2), and catch diode (D3) for shorted junctions. If any component is found shorted, replace it.

C. Preliminary Check on Major Secondary Components.
Using ohmmeter from output common to each output, with output loads disconnected, check for shorted rectifiers or capacitors. If +12V output is shorted, also check crowbar SCR (SCR1).

D. Check for B+ with the fuse intact.
Connect power supply and attach X10 scope probe ground to the anode of (D1). Slowly turn up power and check for B+ on end of R14 nearest the transformer. With imput at 95 VAC, this point should be between 260-270 VDC. If this is not correct, check resistor and and DB1.

If R14 is open it was most likely caused by a shorted component that is fed power by R14. Check the following components for proper operation (Q2, Q1, D1, D36).

E. Check Q2 Waveforms
Using X10 probe on heat sink of Q2, check collector waveform. Transistor should be switching, correct waveform is shown in Figure 5. If this is not present, check for open junction on Q2. If OK check to see if base voltage is being supplied to Q2, it should be .7V. If it is not present, check components (L3, Q1, D1, and R4).

Section IV

LOW OUTPUT

A. All outputs are low.
If all outputs are low at the same time, check to ensure that the voltage slection jumper is in the proper position.

B. +5V AND +12V -2 outputs
The power supply regulates off of the +5V and +12V -2 outputs. If these outputs are low, it could cause the others to be low. If so, adjust +5V and +12V -2 outputs by removing or adding R27 and R28.

C. If any one output is not present, first check the rectifier associated with that output and then the rest of the components in the circuit and the solder joints on the PCB.

Section V

CROWBAR

If the crowbar is not operating, Check Z1, and SCR1. If the crowbar is not triggering within the specified limits change Z1.

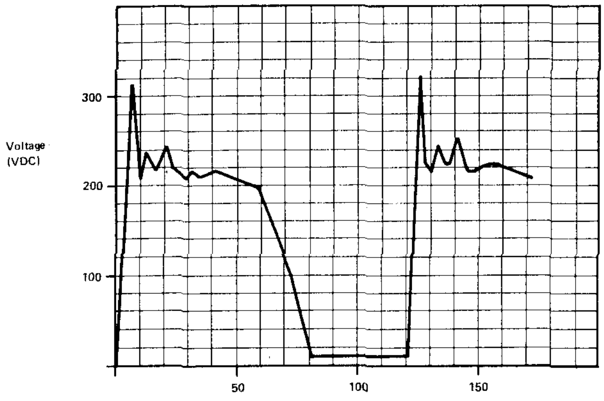


Figure 5. Q2 Collector Waveform

Section VI

Performance Test

Each of these test conditions should be set-up and noted to be within the limits. If the power supply does not pass the above tests, refer to Section IV and V.

Troubleshooting the Power Supply -Secondary Drive
Section 1

Equipment for Test Set-Up

1. Isolation Transformer (minimum of 500 VA rating)-

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0-280 Variable Transformer (Variac)-
   Used to vary input voltage. Recommend 10 Amp, 1.4 KVA rating minimum.

3. Voltmeter-
   Needed to measure DC voltages to 50 VDC and AC voltages to 400 VAC. Recommend two digital multimeters.

4. Oscilloscope-
   Need X10 probe.

5. Load Board with Connectors-
   See Table 2 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

6. Ohmmeter

7. Wattmeter

Set-Up Procedure

Set-up as shown in Figure 6. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 50mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of Section III for test points within power supply.

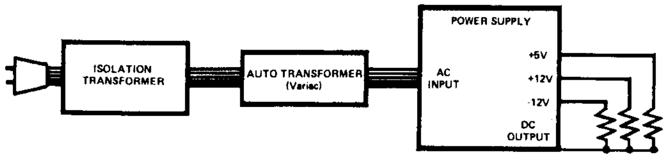


Figure 6. Test Set-Up

Section II

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

LOAD BOARD VALUES

OUTPUT	MIN LOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5	0.45A	11.11 ohm	5W	2.5A	2 ohm	25W
+12	1.3A	0.40 ohm	8W	2.02A	24.24 ohm	50W
-12	0	0	0	0	120 ohm	2W

Table 2. Load Board Values

Start-Up

First note the position of the input voltage select wire. this wire can be found at the end of PCB opposite the input/output connectors.Make sure wire is in position corresponding to your test set-up 230V position if you are using 115V input. For the balance of this troubleshooting section we will assume 230V operation. If you prefer 115V operation divide applicable values in half.

Load power supply with minimum load as specified in Table 2. Bring power up slowly with Variable Transformer while monitoring +5 output with scope and DVM and input with DVM and wattmeter. If the wattmeter shows significant power with low AC power being applied, shut down and refer to Section III.. Supply should start with approximately 80-120 VAC applied and should regulate when 190 VAC is applied. If output has reached +5 volts, do a performance test as shown in Section IV. If there is no output, refer to Section III.

Section III

NO OUTPUT

A. Check Fuse
If fuse is blown, replace it, but do not apply power until the cause of failure is found.

B. Preliminary Check on Major Primary Components
Check thermistor (R1), diode bridge (DB1), power transistor (Q2), and catch diode (D3) and turn-off transistor (Q1), emitter resistor (R10), and diode (D1) for shorted junctions. If any component is found shorted, replace it.

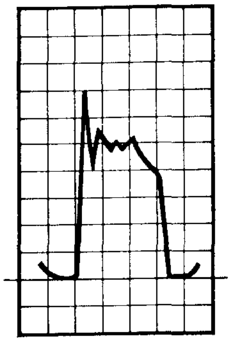
C. Preliminary Check on Major Secondary Components.
Using ohmmeter from output common to each output, with output loads disconnected, check for shorted rectifiers or capacitors. If +12 output is shorted, also check crowbar SCR (SCR1) and zener (Z1).

D. Check for B+

Setup power supply and attach X10 scope probe ground to end of R11 closest to input capacitors. Slowly turn up power and check for B+ on the (+) terminal of the diode bridge (DB1). With input at 95 VAC, this point should be between 120-140 VDC. If this is not correct, check fuse, thermister (R1), DB1, and if necessary, check R2, D3, and finally input capacitors C6 and C7.

E. Check Q2 Waveforms
Using X10 probe on the case of T03 package of Q2, check collector waveform. Transistor should be switching, correct waveform is shown in Figure 7. If this is not present, check for shorted junction on Q2.

If OK check the base waveform. Base of Q2 is the uppermost of the two center leads on the back of Q2 heat sink. The correct waveform is shown in Figure 8. If this waveform is not present, check L3, Q1, and D1, and secondary components Q3, D11, D12, D5, and L4. If any of the semiconductors are found shorted, or inductors open, replace them.



50 V/DIV
5 μsec/DIV

Input – 120VAC
Loads – +5 @ 2A
+12 @ 1A
-12 @ 0.1A

Figure 7. Q2 Collector Waveform

1.0 V/DIV
5 μsec/DIV

Input and Loads same as above.

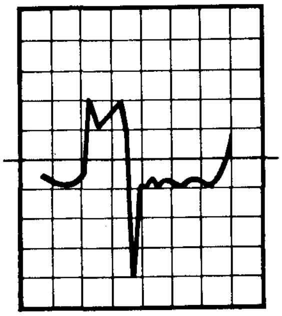


Figure 8. Q2 Base Waveform

Section IV

Performance Test

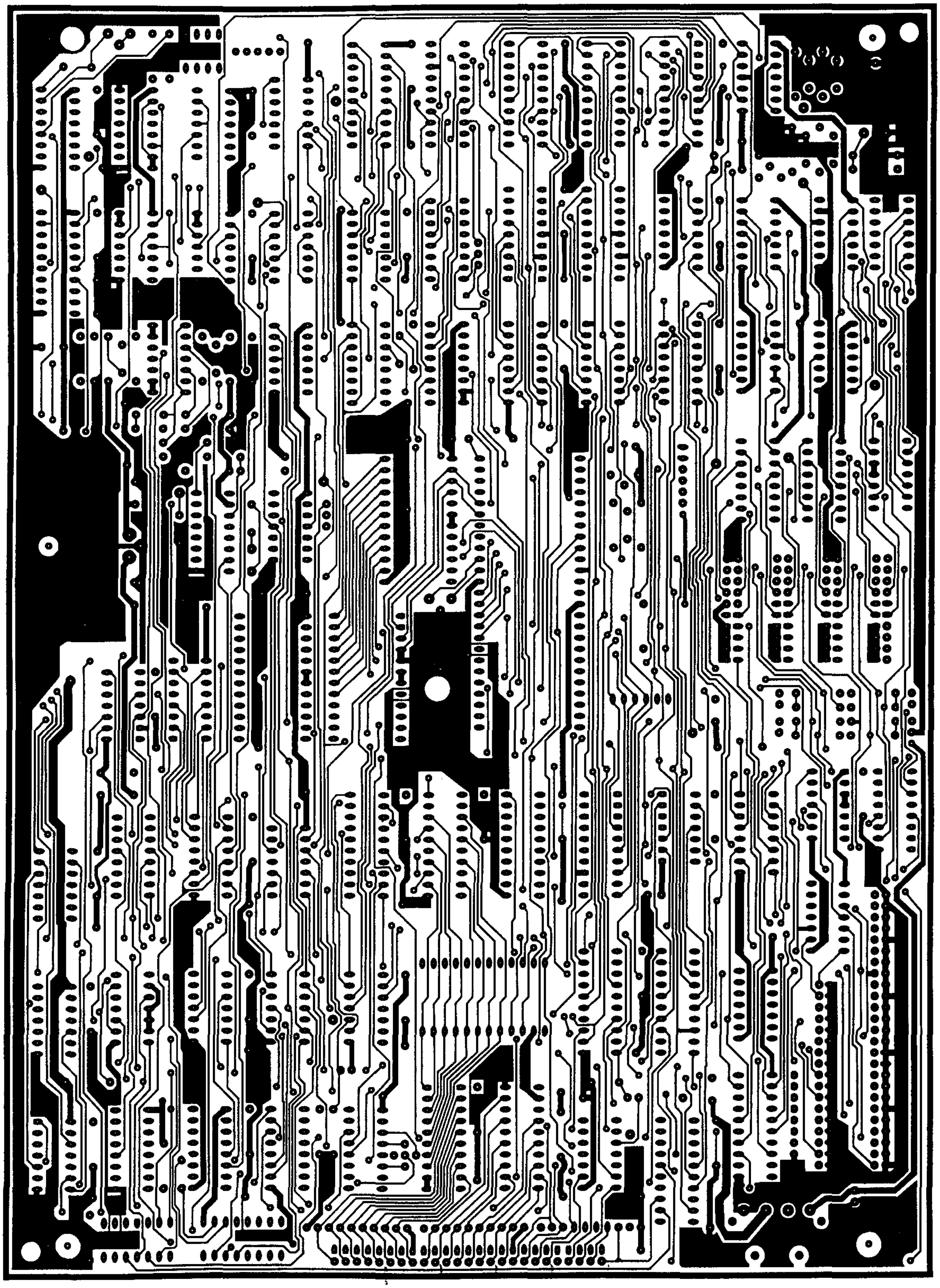
Each of these test conditions should be set-up and noted to be within the limits.

Test	Input	+5 Load	+12 Load	-12 Load
1	95VAC	Max	Max	Max
2	128VAC	Max	Max	Max
3	120VAC	Max	Min	Min
4	128VAC	Min	Min	Min
5	95VAC	Min	Min	Min

VOLTAGE AND RIPPLE SPECIFICATION

OUTPUT	MIN	MAX	NO LOAD	RIPPLE
+5	4.75V	5.25V	-	50mV P-P
+12	11.40V	12.60V	-	150mV P-P
-12	-11.00V	15.00V	-	150mV P-P

* Applies to resistive load only. Not under system operating conditions.



REDUCE TO 12.000±.005

REDUCE TO 9.000±.005

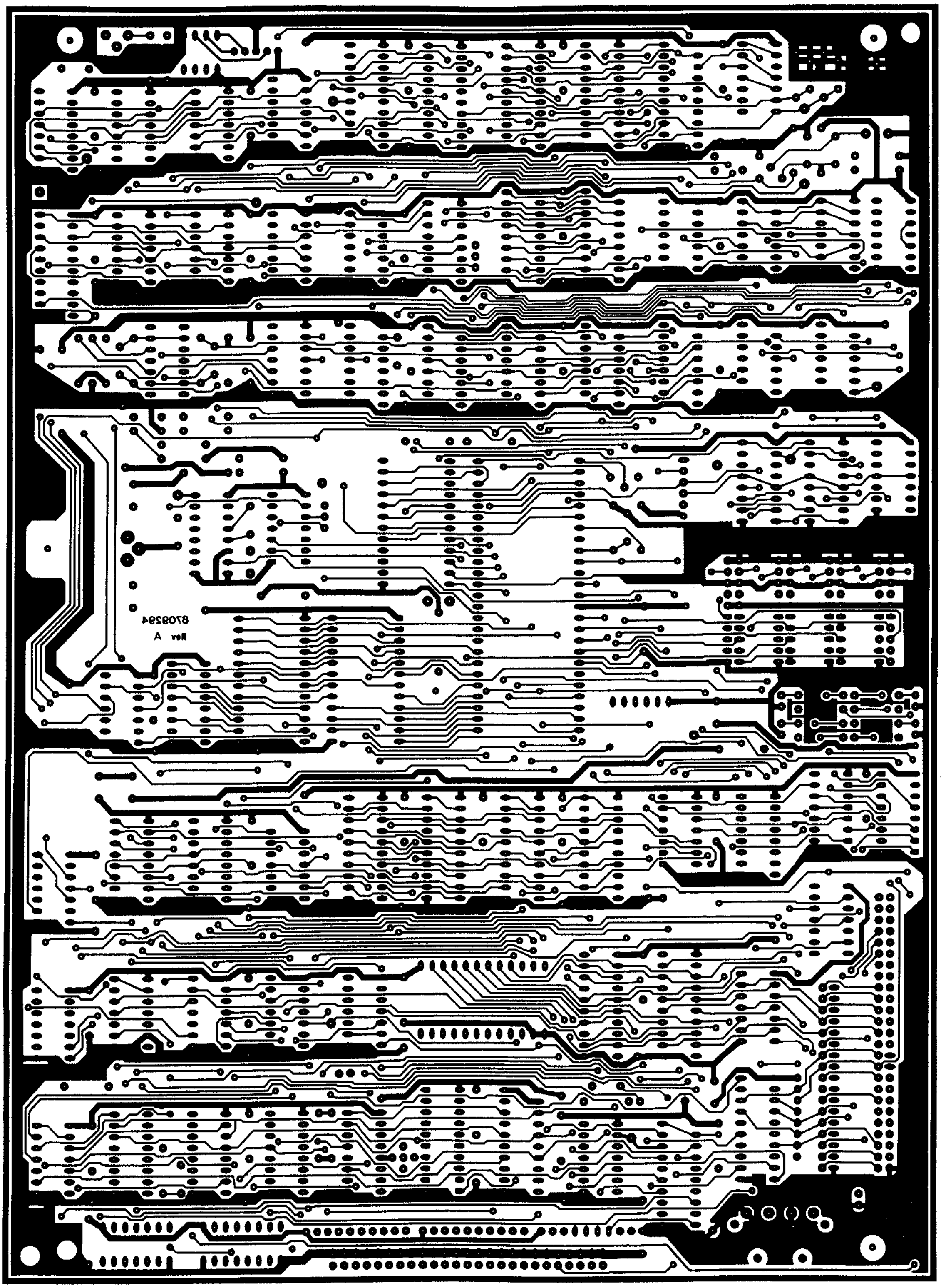
TANDY CORP.

COMPONENT SIDE

1700189
REV A

CONTROLLER BOARD

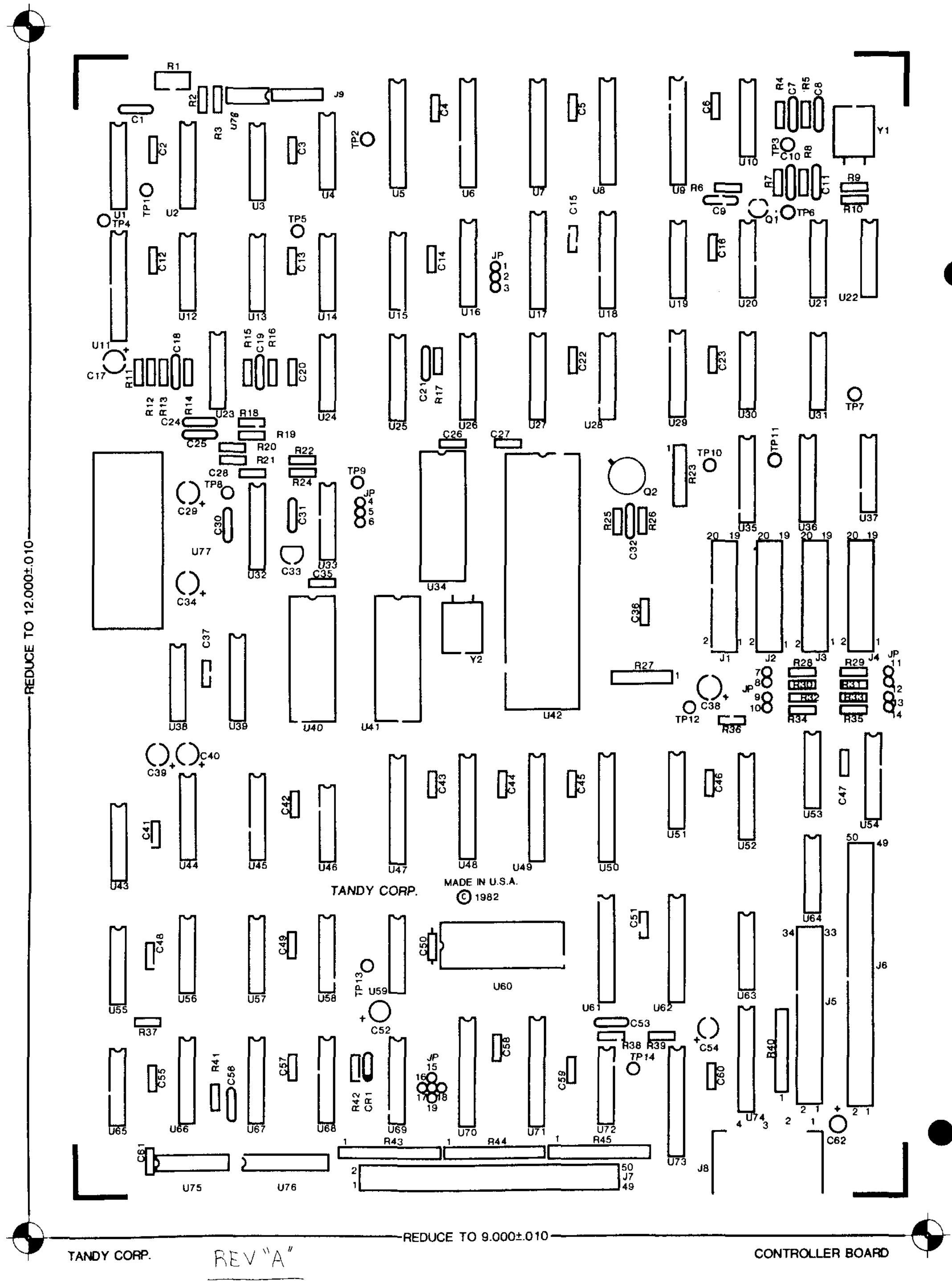
REDUCE TO 12.000±.005

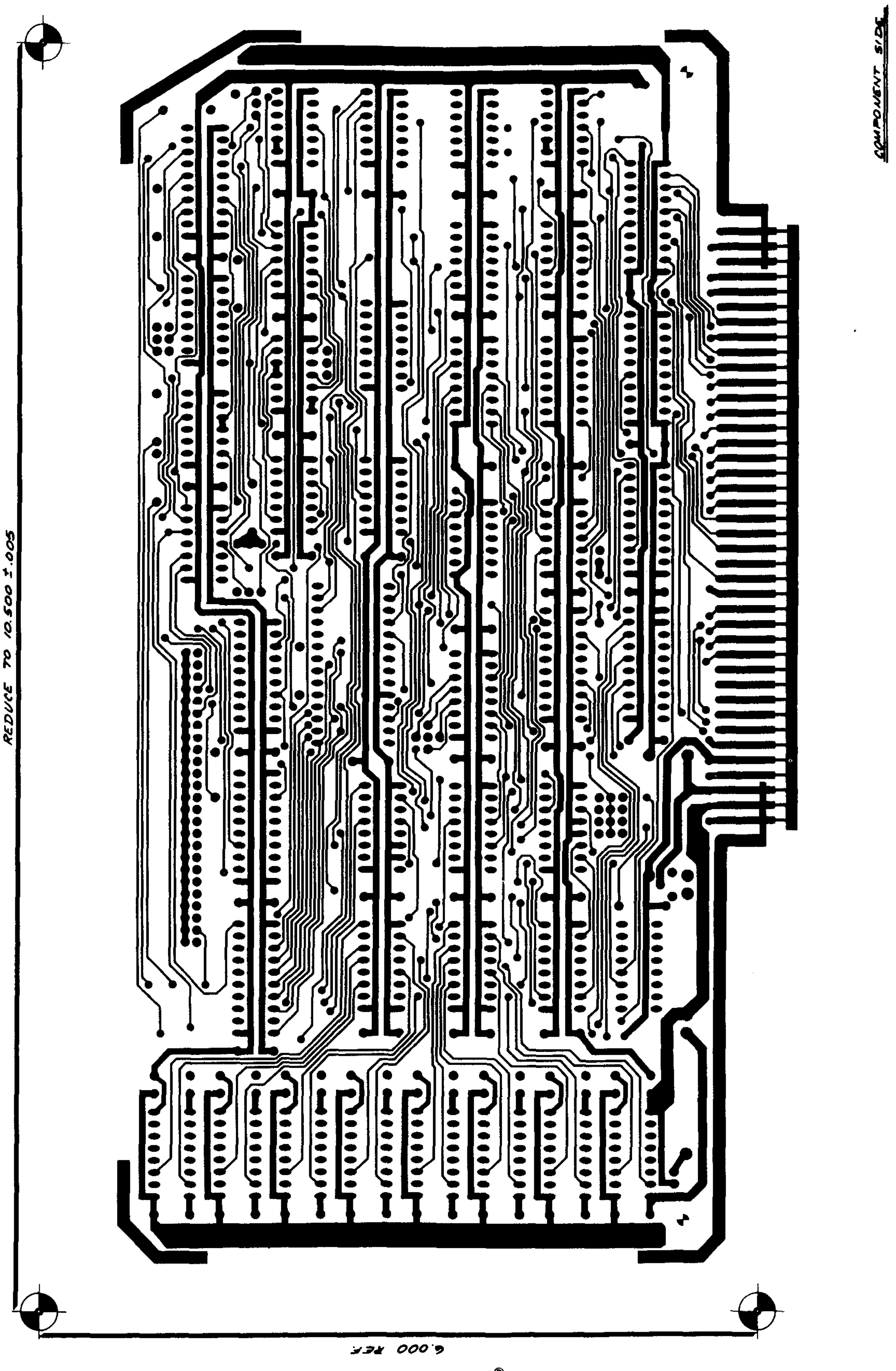


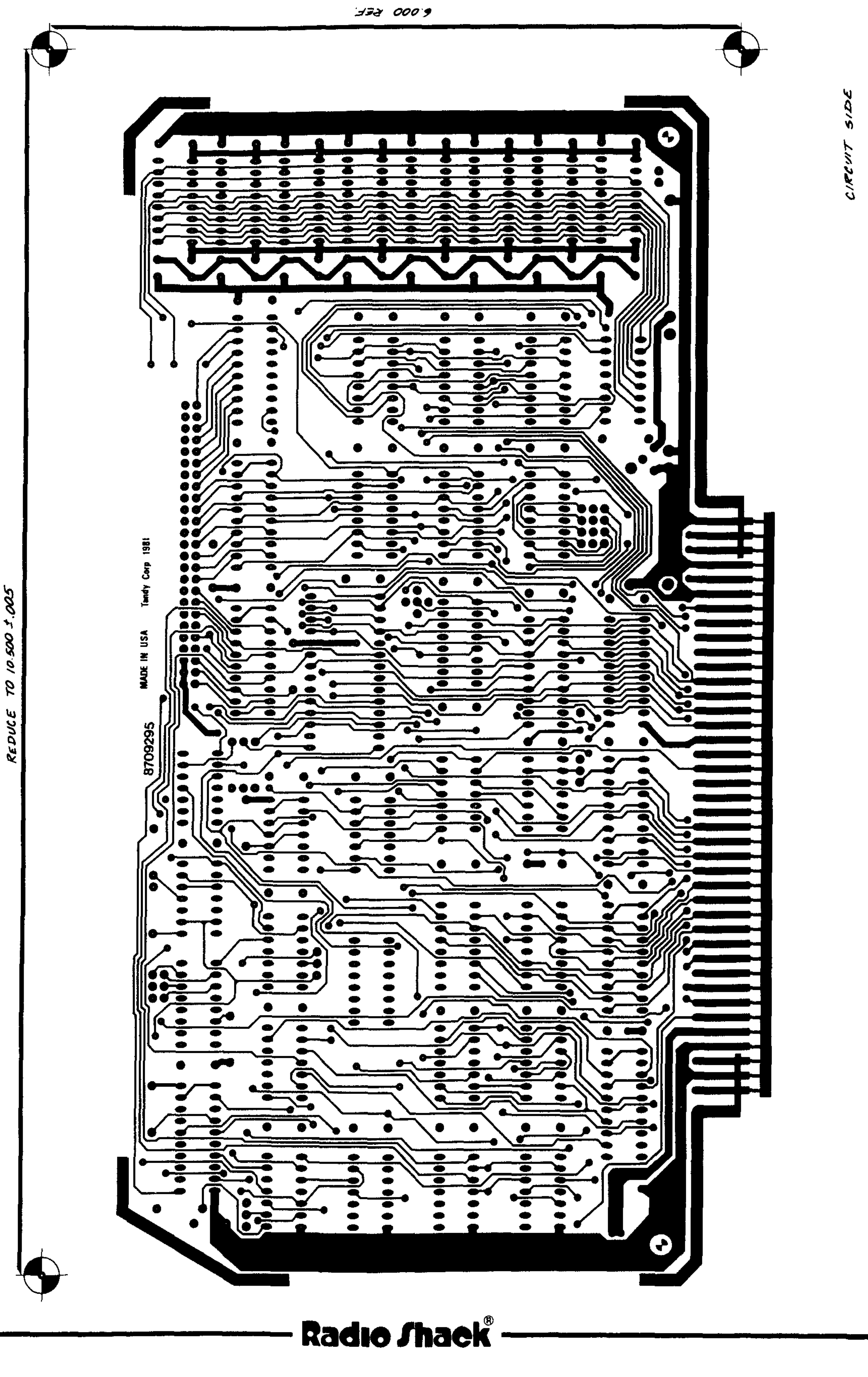
REDUCE TO 9.000±.005

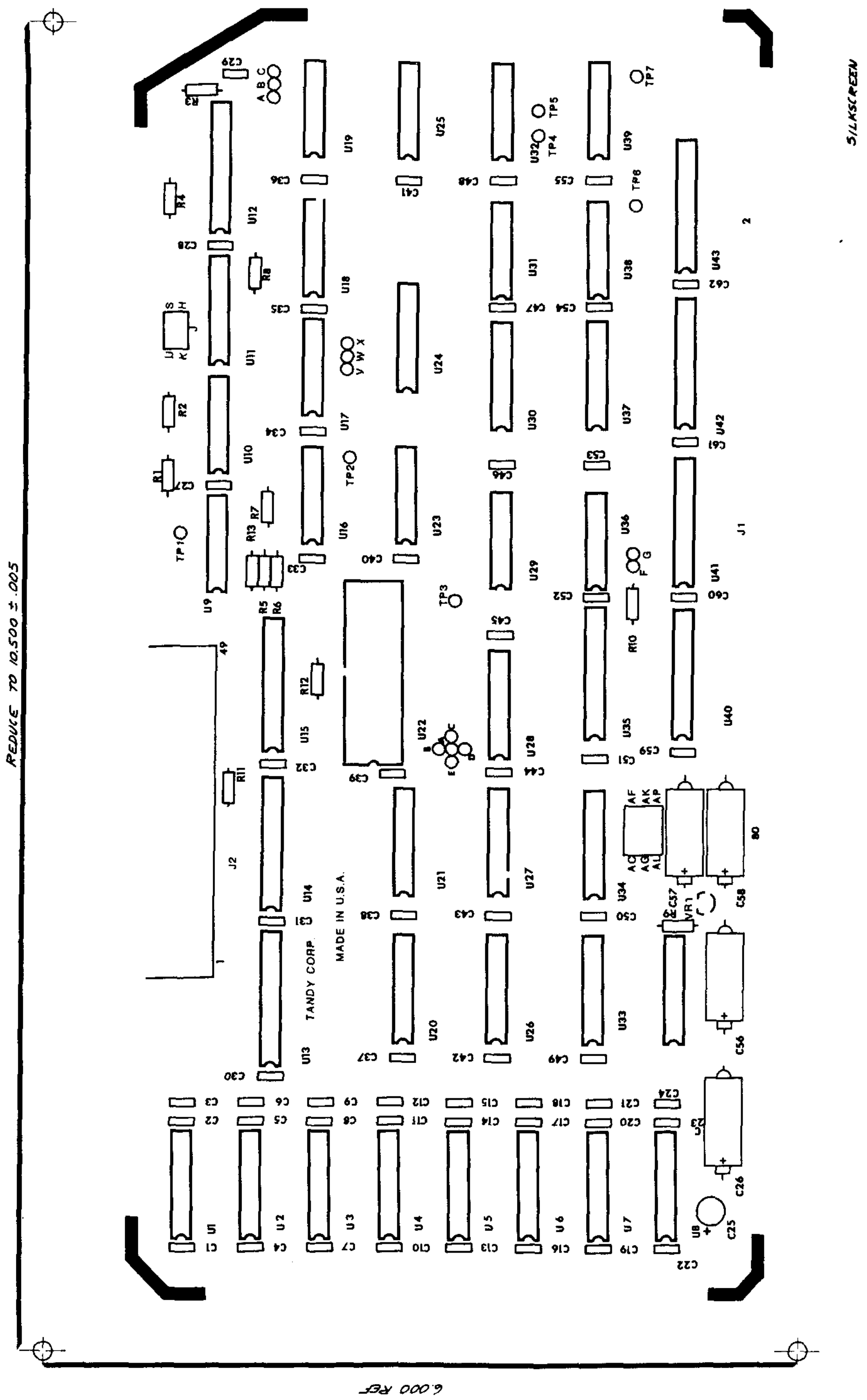
TANDY CORP. CONTROLLER BD SOLDER SIDE 1700189 TANDY CORP. CONTROLLER BOARD

REV A

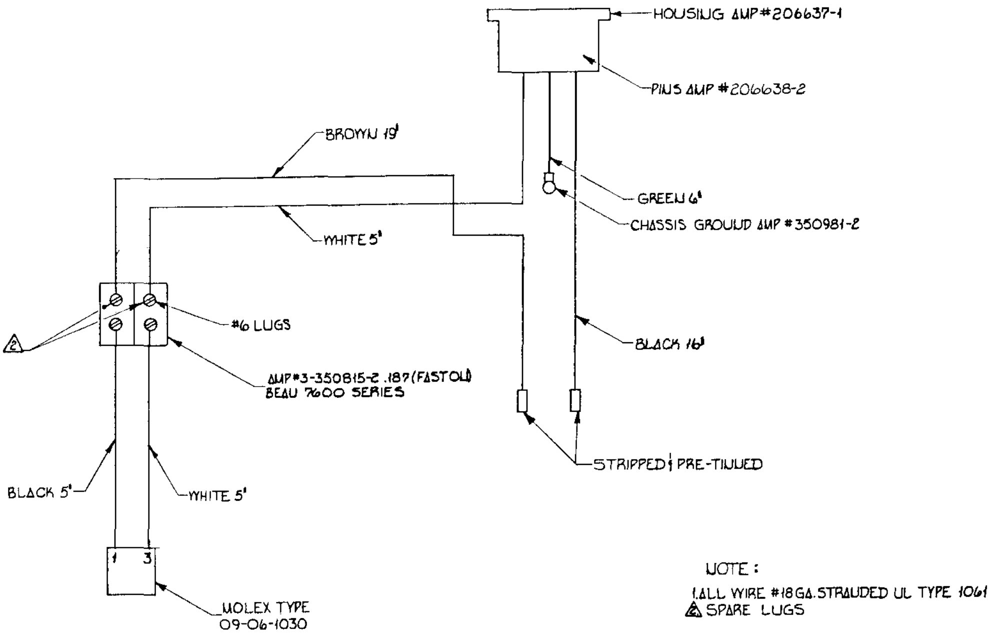

REDUCE TO 12.000±.010
REDUCE TO 9.000±.010
TANDY CORP.
MADE IN U.S.A.
© 1982
TANDY CORP.
REV "A"
CONTROLLER BOARD


COMPONENT SIDE
REDUCE TO 10.500 ±.005
6.000 REF

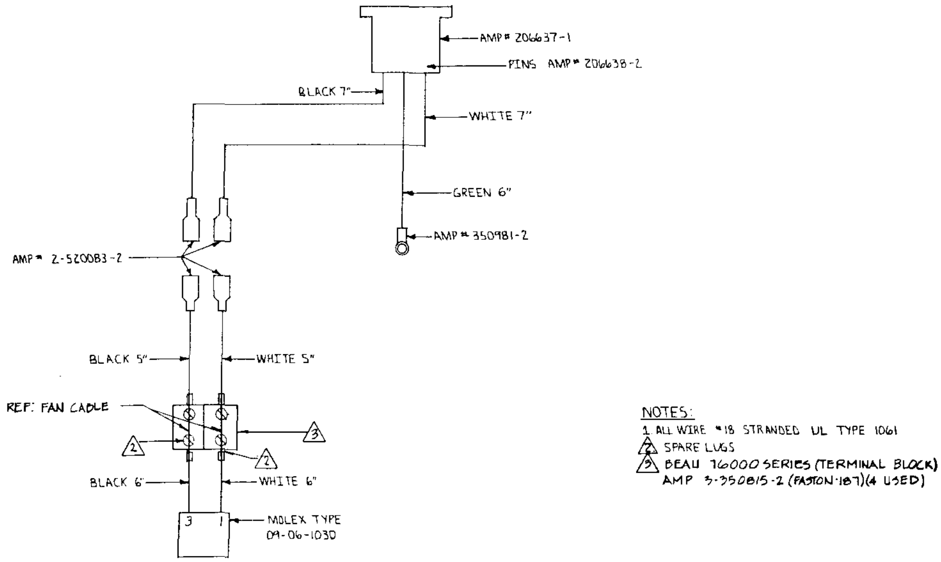

6.000 REF
CIRCUIT SIDE
REDUCE TO 10.500 ±.005
8709295
MADE IN USA
Tandy Corp 1981



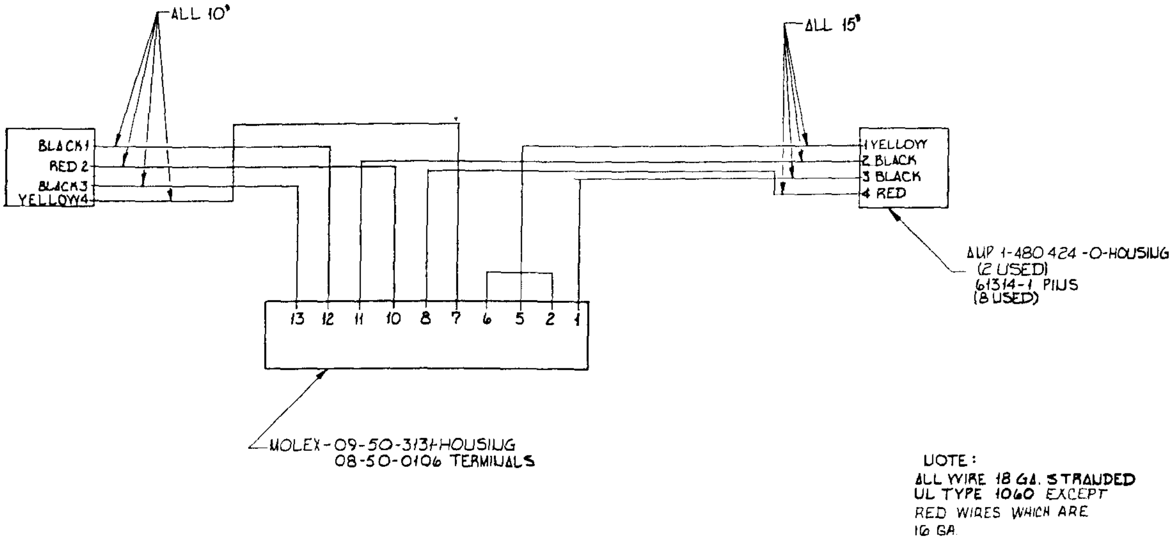
11/ Wiring Diagrams



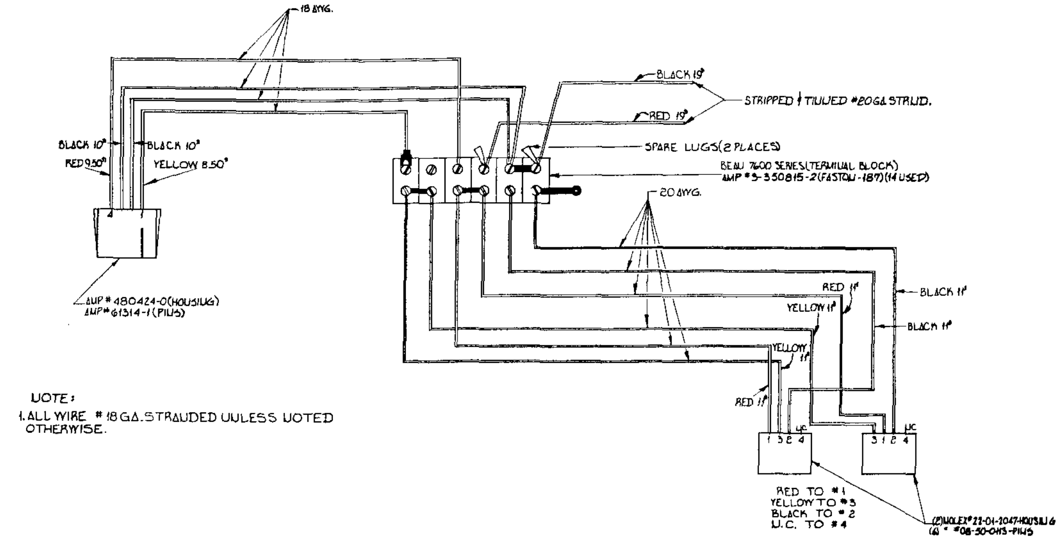
AC Wiring Harness (Primary/Master)



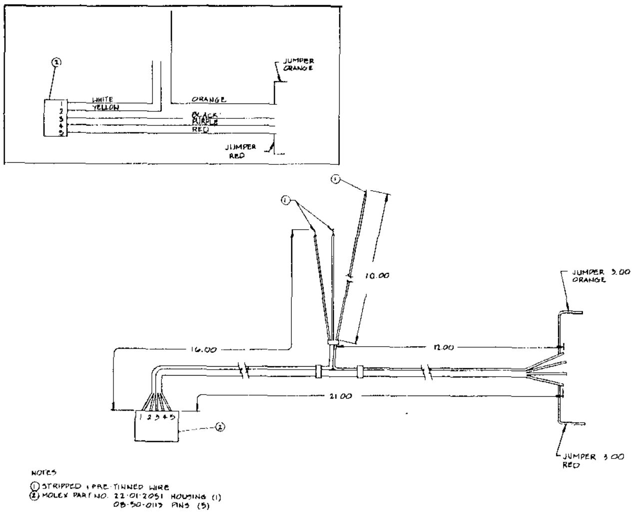
AC Wiring Harness (Secondary/Slave)



DC Power Harness (Primary/Master)

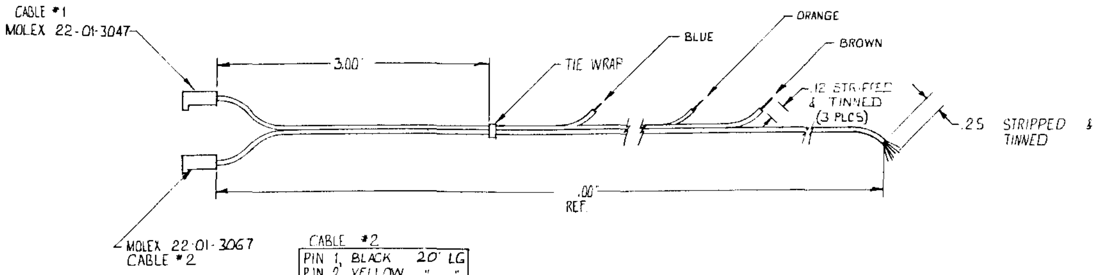


DC Power Harness (Secondary/Slave)



Lamp Driver Wiring Harness (Primary)

CABLE #1		
PIN 1,	BLUE	10
PIN 2,	N/C	
PIN 3,	ORANGE	14
PIN 4,	BROWN	15



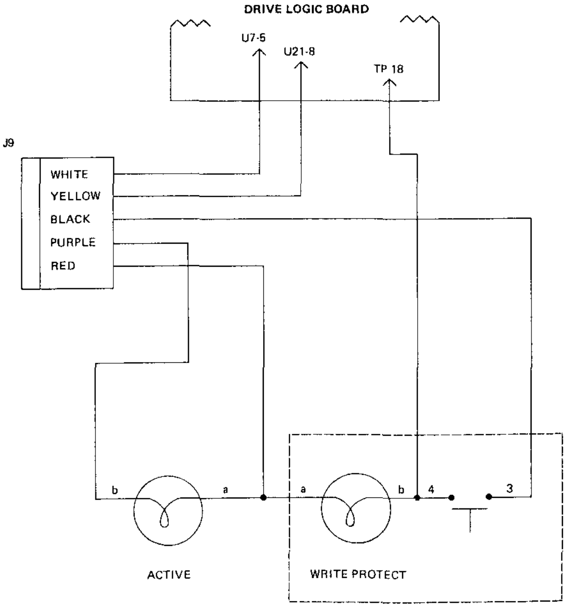
CABLE #2		
PIN 1,	BLACK	20" LG
PIN 2,	YELLOW	" "
PIN 3,	VIOLET	" "
PIN 4,	WHITE	" "
PIN 5,	N/C	" "
PIN 6,	RED	" "

LED Driver Board Harness (Secondary)

NOTES:
1. DIMENSIONS GIVEN REPRESENT TRUE LENGTH OF WIRES. RADUII & ANGLES SHOWN ARE FOR DRAWING REF. ONLY.

Standard Jumpers on Controller Board

17 - 19   1 - 2   5 - 6



FRONT PANEL SWITCH WIRING

12/ Parts Lists

PRODUCT DESCRIPTION
HARD DISK 5 1/4"
CAT. NO. 26-4152

QTY	DESCRIPTION	PART NUMBER
1	MANUAL, START-UP	8749389
1	REFERENCE, MANUAL	8749394
1	MANUAL ASSY	8898419
1	LABEL, TOP H.D. CONN	8789613
1	CORD, 8' POWER*	8709057
1	CABLE, EXT	8709244
1	KIT, ACCESSORY HDM	8898418
1	CASE, BOTTOM*	8729124
1	PLUG, 2 1/2" DIA.	8729148
1	LABEL, FCC PART 15	8789287
1	LABEL, FCC ID HDM	8789808
1	LABEL, S/N	8789790
4	FOOT	8590123
4	WASHER, 1/2 O.D	8589074
4	SCREW, #10 X 1/2"*	8569062
3	PLATE, COVER	8729147
6	SCREW, #4X1/4 PPH	8569120
1	CABLE, INT. CNTRL	8709330
1	CABLE, INT.CNTRLR	8709331
2	SCREW, #6 X 5/16	8569130
2	SCREW, #4-40 X 3/4"PPH	8569059
2	NUT, LOCK #4-40	8579003
2	WASHER, STAR #4	8589075

1	HARNESS, AC MSTR	8709332
1	SCREW, #6-32 X 1/4 (GRD)	8569098
2	SCREW, #4-40 X 1/2"PPH	8569033
2	NUT, LOCK #4-40	8579003
1	FAN, COOLING*	8790401
2	TAB, FASTON	8529008
4	NUT,#6-32 KEPS	8579004
1	FAN, 5M S/A	8896620
1	BEZEL, SWITCH*	8719230
1	SWITCH, KEYLOCK*	8489047
1	SWITCH, ON/OFF*	8489048
1	INDICATOR LIGHT*	8469009
1	BEZEL ASSY	8896610
1	DRIVE, 12 MEG HARD	8790203
4	METAL SLEEVE	8589076
1	HARNESS, LAMP	8709347
2	MOUNT, DRIVE	8729179
4	WASHER, LOCK #6	8589018
4	SCREW, #6-32 X 1/4 PPH	8569098
4	GROMMET, RUBBER	8590127
1	DRIVE, S/A	8896609
1	FILTER	8739010
4	NUT,LOCK #6-32	8579004
4	SCREW, #6-32 X 2 F.CNTSK	8569155
2	SCREW, #6-32 X 1/2	8569126
2	SCREW, #6-32 X 1/4 THD FM	8569040
4	SCREW #6-32 X 1/4"PPH	8569098
4	WASHER, #6	8589018
1	CLIP, CORD .52" DIA.	8559015
1	CLIP, CORD .38" DIA.	8559010
7	TUBING 1/8DX1/2	8539025
1	PCB ASSY, CONTROLLER* (See pages 71-74)	8896130
2	IC P2114 U17, U18	8042114
1	IC, 8X300 MICRO-CONT	8040300
1	IC 28S86 BPROM (U34)PRGMD	8896603
1	IC, 28S86 BPROM (U40)PRGMD	8896602
1	IC, 28S86 BPROM (U41)PRGMD	8896604

1	IC, WD 1100-01 (U9)	8040111
1	IC, WD 1100-12 (U5)	8041112
1	IC, WD 1100-03 (U11)	8040113
1	IC, WD 1100-04 (U6)	8040114
1	IC, WD 1100-05 (U7)	8040115
1	PCB, CONTROLLER 5M F/A	8896600
1	POWER SUPPLY*	8729180
1	INSULATOR	8539026
1	POWER, SUPPLY	8790043
4	SCREW, #6-32 X 1/4"PPH	8569160
4	WASHER, #6 LOCK	8589018
2	SCREW, #10 X 1/4"PH	8569153
1	WASHER, .141 1DX .167 OD	8589072
5	SCREW, #6-32X3/8"PPH	8569003
1	POWER SUPPLY S/A	8896608
1	HARNESS DC MSTR	8709334
4	SCREW, #6-32X1/4 PPH	8569160
4	WASHER, #6 LOCK	8589018
1	HOLDER, PLASTIC MAP	8590109
1	CABLE, INT. DATA MSTR	8709324
1	COVER, TOP	8729123
2	CLIP, GRD.	8559040
5	SCREW, #8-32X3/8"	8569107
5	WASHER, #8 FLAT	8589027
1	LOGO STRIP*	8719221
1	BEZEL*	8719209
1	COVER, TOP S/A	8898403
3	SCREW, #6-32X3/8" PPH	8569026
1	LABEL, LINE TERMINATOR	8789597
1	MANUAL, SERVICE	8749403
1	PCB ASSEMBLY, INTERFACE (See pages 75 and 76)	8898417

PRODUCT DESCRIPTION
5 1/4" HARD DISK
CAT. NO. 26-4153

QTY	DESCRIPTION	PART NUMBER
1	CABLE, EXT. DATA 20POS.	8709384
1	CABLE, EXT. CNTRL 34POS.	8709329
1	CORD, 8' POWER*	8709057
1	CABLE, INT. DATA 20 POS	8709326
1	KIT, ACCESSORY HDS	8898507
1	CASE BOTTOM*	8729181
1	LABEL, FCC PART 15	8789287
1	LABEL, FCC ID HDS	8789809
4	FOOT	8590123
4	SCREW, #10 X 1/2"	8569062
4	WASHER, 1/2 O.D.	8589074
1	LABEL, S/N	8789793
1	CABLE, INT CNTRLR	8709325
1	CABLE, INT. CNTRL/SLV	8709328
2	SCREW, #6 X 5/16 BRICO IND.	8569130
2	SCREW, #4-40X3/4 PPH	8569059
2	NUT,#4-40 KEPS LOCK	8579003

2	WASHER, #4 STAR	8589075
1	FAN, COOLING	8790401
2	TAB, FASTON	8529008
1	FAN, 12M S/A	8896620
4	SCREW, #6-32 X 2" FCNTR	8569155
1	FILTER	8739010
4	NUT, #6-32 LOCK*	8579004
1	HARNESS, AC SLV	8709333
2	SCREW, #4-40 X 1/2"PPH	8569033
2	NUT, LOCK #4-40	8579003
1	BEZEL, SWITCH*	8719230
1	INDICATOR, PWR ON	8469011
1	SWITCH, ON/OFF*	8489048
1	INDICATOR LIGHT*	8469009
1	BEZEL ASSY	8896611
1	HARNESS DC ASSY	8709335
1	RELAY, 12V 70MA	8429104
4	SCREW, #6-32 X 1/2	8569126
2	SCREW, #6-32 X 1/4	8569098
2	SCREW, #6-32 X 1/2	8569152
2	SCREW, #6-32 X 3/8	8569026
2	CLIP CORD .38 DIA.	8559010
7	TUBING 1/8 DIA. X 1/2	8539025
1	DRIVE, 12 MEG HARD	8790203
1	HARNESS, LED DRIVER	8709348
1	HARNESS, RELAY	8709355
2	MOUNT, DRIVE	8729179
4	SCREW, #6-32 X 1/4 PPH	8569003
1	DRIVE, 12M HDS S/A	8898422
1	POWER SUPPLY	8790025
9	SCREW. #6-32 X 1/4 PPH	8569160
1	SCREW, #6-32X1 PPH ZINC	8569159
2	NUT, #6-32 KEPS	8579004
1	PCB DRIVER F/A 12M	8896615

1	HOLDER, PLASTIC MAP	8590109
1	COVER, TOP	8729123
2	CLIP, GRD.	8559040
3	SCREW, #6-32 X 3/8 PPH	8569026
5	SCREW, #8-32 X 3/8	8569107
5	WASHER, #8 FLAT	8589027
1	LOGO, STRIP	8719259
1	BEZEL	8719209
1	LABEL, WARRANTY NOT.	8789090
1	BAG, 6X15X22	8590124
1	LABEL, LINE TERMINATOR	8789597

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(8896130)
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SYMBOL	QTY	DESCRIPTION	PART NO.
	1	PCB LOGIC BOARD REV. " - "	8709294
TP1-14	14	STAKING PINS	8529014
C1	1	CAPACITOR 68 PFD 50V C. DISK	8300683
C2-6	5	CAPACITOR .1 MFD 50V MONO	8374104
C7-9	3	CAPACITOR 100 PFD 50V C. DISK	8301104
C10	1	CAPACITOR 68 PFD 50V C. DISK	8300683
C11	1	CAPACITOR 22 PFD 50V C. DISK	8300224
C12-16	5	CAPACITOR .1 MFD 50V MONO	8374104
C17	1	CAPACITOR 100 MFD 16V ELEC. RAD.	8327101
C18,19	2	CAPACITOR 10 PFD 50V C. DISK	8300104
C20	1	CAPACITOR .1 MFD 50V MONO	8374104
C21	1	CAPACITOR 68 PFD 50V C. DISK	8300683
C22,23	2	CAPACITOR .1 MFD 50V MONO	8374104
C24	1	CAPACITOR .0068 MFD 50V POLY	8302684
C25	1	CAPACITOR 150 PFD 50V C. DISK	8301153
C26-28	3	CAPACITOR .1 MFD 50V MONO	8374104
C29	1	CAPACITOR 10 MFD 16V ELEC. RAD.	8326101
C30	1	CAPACITOR 330 PFD 50V C. DISK	8301332
C32	1	CAPACITOR 100 PFD 50V C. DISK	8301104
C33	1	CAPACITOR 6-50 PF TRIM NPO	8360550
C34	1	CAPACITOR .47 MFD 16V ELEC. RAD.	8324471
C35-37	3	CAPACITOR .1 MFD 50V MONO	8374104
C41-51	11	CAPACITOR .1 MFD 50V MONO	8374104
C52	1	CAPACITOR 2.2 MFD 25V ELEC. RAD.	8325221
C53	1	CAPACITOR 100 PFD 50V C. DISK	8301104
C54	1	CAPACITOR 100 MFD 16V ELEC. RAD.	8327101
C55	1	CAPACITOR .1 MFD 50V MONO	8374104
C56	1	CAPACITOR .01 MFD 50V C. DISK	8303104
C57-61	5	CAPACITOR .1 MFD 50V MONO	8374104
C62	1	CAPACITOR 47 MFD 16V ELEC. RAD.	8326471
CR1	1	DIODE IN4148	8150148
J1-4	4	CONNECTOR 20-PIN HEADER (SIP)	8519121
J5	1	CONNECTOR 34-PIN HEADER (SIP)	8519120
J7	1	CONNECTOR 50-PIN HEADER (SIP)	8519117
J8	1	CONNECTOR 4-PIN RIGHT ANGLE (POWER)	8519141
J9	1	CONNECTOR 5-PIN HEADER (SIP) STRAIGHT	8519145
JP1-6	6	JUMPERS	8529014
JP15-19	5	JUMPERS	8529014
Q1	1	TRANSISTOR MPS2907	8100907
Q2	1	INSULATOR, TRANSISTOR	8
Q2	1	TRANSISTOR 2N5320	8110320

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(8896130)
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SYMBOL	QTY	DESCRIPTION	PART NO.
R1	1	TRIM POT 10K OHM MULTITURN	8279311
R2,3	2	RESISTOR 2K OHM 1/4 WATT 5%	8207220
R4-6	3	RESISTOR 560 OHM 1/4 WATT 5%	8207156
R7	1	RESISTOR 270 OHM 1/4 WATT 5%	8207127
R8	1	RESISTOR 510 OHM 1/4 WATT 5%	8207151
R9,10	1	RESISTOR 27K OHM 1/4 WATT 5%	8207327
R11,12	2	RESISTOR 100 OHM 1/4 WATT 5%	8207110
R13	1	RESISTOR 270 OHM 1/4 WATT 5%	8207127
R14,15	2	RESISTOR 620 OHM 1/4 WATT 5%	8207162
R16	1	RESISTOR 2K OHM 1/4 WATT 5%	8207220
R17	1	RESISTOR 43K OHM 1/4 WATT 5%	8207343
R18,19	2	RESISTOR 100 OHM 1/4 WATT 5%	8207110
R20	1	RESISTOR 330 OHM 1/4 WATT 5%	8207133
R21	1	RESISTOR 680 OHM 1/4 WATT 5%	8207168
R22	1	RESISTOR 5.6K OHM 1/4 WATT 5%	8207256
R23	1	RESISTOR PAK 1K OHM SIP 6-PIN	8290210
R24	1	RESISTOR 4.7K OHM 1/4 WATT 5%	8207247
R25	1	RESISTOR 560 OHM 1/4 WATT 5%	8207156
R26	1	RESISTOR 10K OHM 1/4 WATT 5%	8207310
R27	1	RESISTOR PAK 4.7K OHM SIP 6-PIN	8293247
R28-35	8	RESISTOR 50 OHM 1/4 WATT 5%	8207051
R36	1	RESISTOR 10 OHM 1/4 WATT 5%	8207010
R37	1	RESISTOR 4.7K OHM 1/4 WATT 5%	8207247
R38	1	RESISTOR 560 OHM 1/4 WATT 5%	8207156
R39	1	RESISTOR 220 OHM 1/4 WATT 5%	8207122
R40	1	RESISTOR PAK 220/330 OHM SIP 8-PIN	8290019
R41	1	RESISTOR 16K OHM 1/4 WATT 5%	8207316
R42	1	RESISTOR 10K OHM 1/4 WATT 5%	8207310
R43-45	3	RESISTOR PAK 220/330 OHM SIP 10-PIN	8290020

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(8896130)
REV. 09/07/82 PAGE 3 OF 4

SYMBOL	QTY	DESCRIPTION	PART NO.
U1	1	IC 26S02 ONE SHOT	8060002
U2	1	IC 74LS193 DUAL CLOCK COUNTER	9020193
U3	1	IC 74S74 DUAL FLIP-FLOP	9010074
U4	1	IC 74S51 AND OR INVERTER	9010051
U5-7	3	SOCKET 20-PIN (DIP)	8509009
U8	1	IC 74LS244 LINE DRIVERS	9020244
U9	1	SOCKET 20-PIN (DIP)	8509009
U10	1	IC 74S74 DUAL FLIP-FLOP	9010074
U11	1	SOCKET 20-PIN (DIP)	8509009
U12-14	3	IC 74S74 DUAL FLIP-FLOP	9010074
U15	1	IC 74S86 QUAD 2-IN OR	9010086
U16	1	IC 74LS175 QUAD FLIP-FLOP	9020175
U17	1	SOCKET 18-PIN (DIP)	8509006
U18	1	SOCKET 18-PIN (DIP)	8509006
U19	1	IC 74LS14 HEX INVERTER	9020014
U20,21	2	IC 74S74 DUAL FLIP-FLOP	9010074
U22	1	IC 74LS74 DUAL FLIP-FLOP	9020074
U23	1	IC MPQ6700 TRANSISTOR PAK	8180700
U24	1	IC 74LS32 QUAD 2-IN OR	9020032
U25	1	IC 74LS123 DUAL MULTIVIBRATOR	9020123
U26-28	3	IC 74LS191 COUNTER	9020191
U29	1	IC 74LS174 HEX FLIP-FLOP	9020174
U30	1	IC 74S00 QUAD 2-IN NAND	9010000
U31	1	IC DDU4-5060 60NS DELAY LINE	8429016
U32	1	IC 74S124 DUAL OSCILLATOR	9010124
U33	1	IC 74S02 QUAD 2-IN NOR	9010002
U34	1	SOCKET 24-PIN (DIP)	8509001
U35,36	2	IC MC3487 DRIVER	8050487
U37	1	IC 74LS54 AND OR INVERT	9020054
U38	1	IC 74LS08 QUAD 2-IN AND	9020008
U39	1	IC 74S174 HEX FLIP-FLOP	9010174
U40	1	SOCKET 24-PIN (DIP)	8509001
U41	1	SOCKET 24-PIN (DIP)	8509001
U42	1	SOCKET 50-PIN (ZRF)	8509012
U43	1	IC 74LS74 DUAL FLIP-FLOP	9020074
U44,45	2	IC 74S138 LINE DECODER	9010138
U46	1	IC 74S04 HEX INVERTER	9010004
U47	1	IC 74LS273 OCTAL FLIP-FLOP	9020273
U48,49	2	IC 74LS244 LINE DRIVERS	9020244

BILL OF MATERIAL
5 1/4" HARD DISK CONTROLLER PC BOARD ASSY.(8896130)
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SYMBOL	QTY	DESCRIPTION	PART NO.
U50	1	IC 74LS240 OCTAL BUFFER	9020240
U51	1	IC 74LS54 AND OR INVERT	9020054
U52	1	IC 74LS174 HEX FLIP-FLOP	9020174
U53	1	IC 74S64 AND OR INVERTER	9010064
U54	1	IC MC3486 RECIEVER	8050486
U55	1	IC 74LS125 QUAD BUFFER	9020125
U56	1	IC 74S64 AND OR INVERTER	9010064
U57	1	IC 74LS08 QUAD 2-IN AND	9020008
U58	1	IC 74S04 HEX INVERTER	9010004
U59	1	IC 74S08 QUAD 2-IN AND	9010008
U60	1	IC 8T31 TRANSCIEVER	9060031
U61	1	IC 74LS374 OCTAL FLIP-FLOP	9020374
U62	1	IC 74LS273 OCTAL FLIP-FLOP	9020273
U63,64	2	IC 7416 HEX INVERTER	9010016
U65	1	IC 74S32 QUAD 2-IN OR	9010032
U66,67	2	IC 74LS139 DUAL LINE DECODER	9020139
U68	1	IC 74S139 DUAL DECODER	9010139
U69	1	IC 74S138 LINE DECODER	9010138
U70	1	IC 8304 BUS TRANCIEVER	8060304
U71	1	IC 74LS244 LINE DRIVERS	9020244
U72	1	IC 7416 HEX INVERTER	9010016
U73	1	IC 74LS244 LINE DRIVERS	9020244
U74	1	IC 74LS374 OCTAL FLIP-FLOP	9020374
U75	1	IC 74S04 HEX INVERTER	9010004
U76	1	IC 74LS221 DUAL MULTIVIBRATOR	9020221
U77	1	IC 78M05 +5V REGULATOR	8051805
U77	1	SCREW, #4-40 X 3/8" PPH	8569002
U77	1	NUT #4, KEPS	8579003
U77	1	HEAT SINK 6070B	8549011
U78	1	IC 75453 LAMP DRIVER	8050453
Y1	1	CRYSTAL 20.0 MHZ	8409024
Y2	1	CRYSTAL 8.000 MHZ	8409006

BILL OF MATERIAL
5 1/4" HARD DISK INTERFACE PC BOARD ASSY.(8898417)
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SYMBOL	QTY	DESCRIPTION	PART NO.
	1	PC BOARD (INTERFACE) " - "	8509295
TP1-7	7	STAKING PINS	8529014
ABC	3	STAKING PINS	8529014
BCDE,FG	6	STAKING PINS	8529014
HJK,STU	6	STAKING PINS	8529014
VWX	3	STAKING PINS	8529014
AC-AF	4	STAKING PINS	8529014
AG-AK	4	STAKING PINS	8529014
AL-AP	4	STAKING PINS	8529014
C1-24	24	CAPACITOR .1 UF 50V MONO AXIAL	8374104
C25	1	CAPACITOR 10 UF 16V ELEC. RAD.	8326101
C26	1	CAPACITOR 10 UF 16V ELEC. AXIAL	8316101
C27-55	29	CAPACITOR .1 UF 50V MONO AXIAL	8374104
C56	1	CAPACITOR 47 UF 16V ELEC. AXIAL	8316471
C57	1	CAPACITOR 47 UF 16V ELEC. AXIAL	8316471
C58	1	CAPACITOR 33 UF 50V ELEC. AXIAL	8316334
C59-62	4	CAPACITOR .1 UF 50V MONO AXIAL	8374104
J2	1	CONNECTOR 50-PIN RGHT.ANG. LATCH	8519147
R1-3	3	RESISTOR 51 OHM 1/4WATT 5%	8207051
R4	1	RESISTOR 4.7K OHM 1/4WATT 5%	0207247
R5	1	RESISTOR 1K OHM 1/4WATT 5%	8207210
R6	1	RESISTOR 4.7K OHM 1/4WATT 5%	8207247
R7	1	RESISTOR 4.7K OHM 1/4WATT 5%	8207247
R8	1	RESISTOR 100 OHM 1/4WATT 5%	8207110
R9-13	5	RESISTOR 4.7K OHM 1/4WATT 5%	8207247
RP1	1	RESISTOR PAK 39 OHM DIP	8290002
U1-8	8	SOCKET 16-PIN	8509003
U13	1	SOCKET 20-PIN	8509009
U20	1	SOCKET 16-PIN	8509003
U22	1	SOCKET 28-PIN	8509007
U26	1	SOCKET 16-PIN	8509003
U40	1	SOCKET 20-PIN	8509009

BILL OF MATERIAL
5 1/4" HARD DISK INTERFACE PC BOARD ASSY.(8898417)
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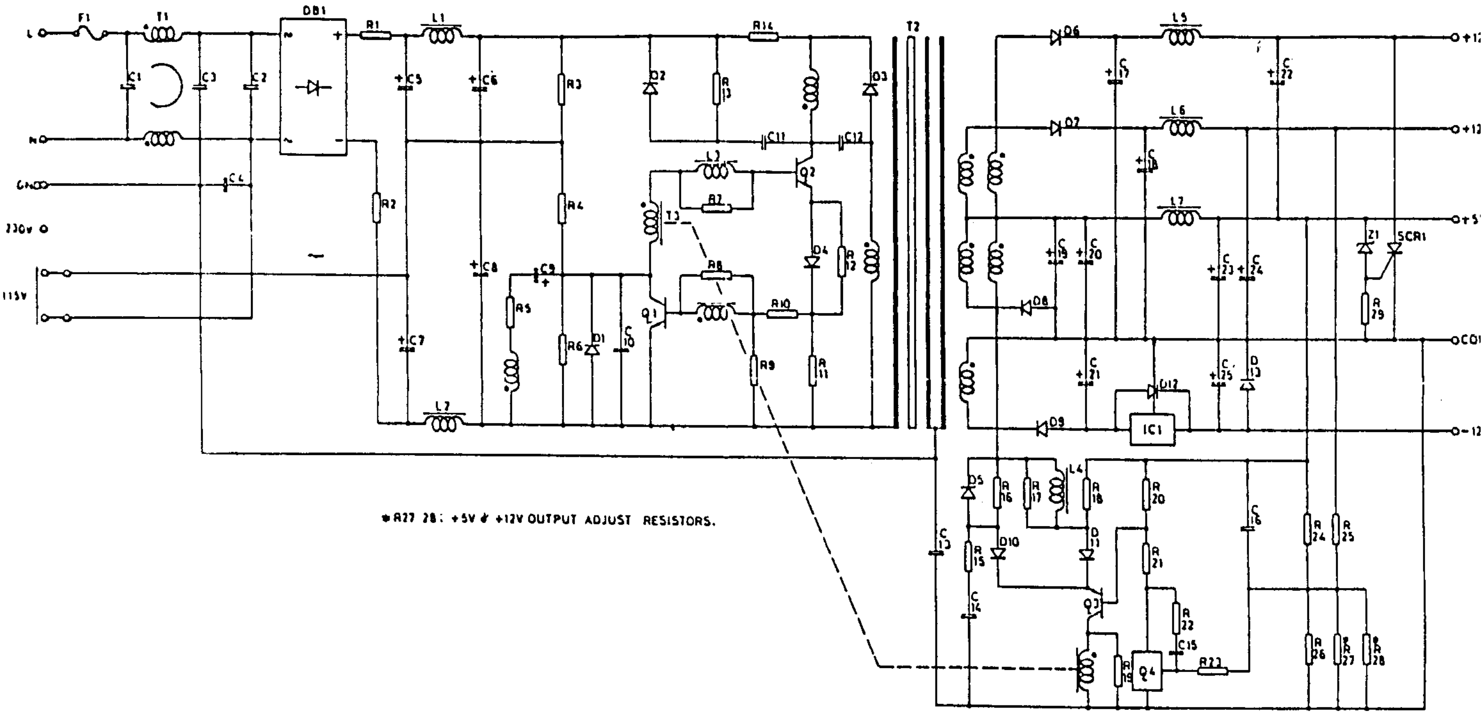
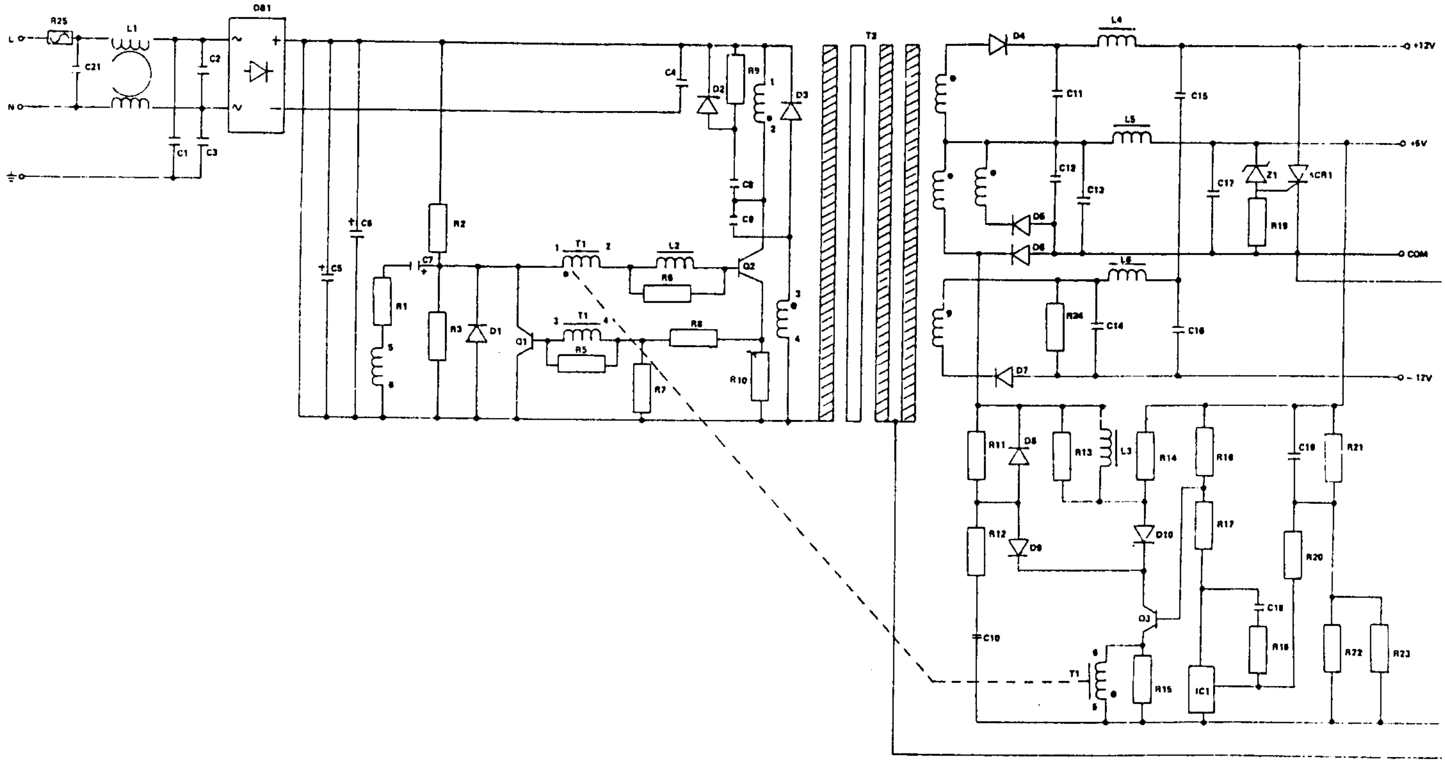
SYMBOL	QTY	DESCRIPTION	PART NO.
U1-8	8	IC MK4116 RAM	8041016
U9	1	IC 74S04 HEX INVERTER	9010004
U10	1	IC 74LS00 QUAD 2-IN NAND	9020000
U11	1	IC DDU-200 DELAY 200 NS	8429004
U12	1	IC 74LS240 OCTAL BUFFER	9020240
U13	1	IC 8304 8 BIT BUS DRIVER	8060304
U14	1	IC 74LS244 OCTAL BUFFER	9020244
U15	1	IC 74LS244 OCTAL BUFFER	9020244
U16	1	IC 74S74 DUAL FLIP-FLOP	9010074
U17	1	IC 74S11 TRIPLE 3-IN AND	9010011
U18	1	IC 74S04 HEX INVERTER	9010004
U19	1	IC 74S00 QUAD 2-IN NAND	9010000
U20	1	IC 8T26 4 BIT BUS DRIVER	9060026
U21	1	IC 74157 QUAD	9000157
U22	1	IC Z80 CTC	8047882
U23	1	IC 74S32 QUAD 2-IN OR	9010032
U25	1	IC 74S02 QUAD 2-IN NOR	9010002
U26	1	IC 8T26 4 BIT BUS DRIVER	9060026
U27	1	IC 74157 QUAD	9000157
U28	1	IC 74S138 DECODER	9010138
U29	1	IC 74S04 HEX INVERTER	9010004
U30	1	IC 74S139 DECODER	9010139
U31	1	IC 74S04 HEX INVERTER	9010004
U32	1	IC 74LS14 HEX INVERTER	9020014
U33	1	IC 74LS174 HEX FLIP-FLOP	9020174
U34	1	IC 74LS138 DECODER	9020138
U35	1	IC 74LS273 FLIP-FLOP	9020273
U36	1	IC 74S08 QUAD 2-IN AND	9010008
U37	1	IC 74LS133 13-IN NAND	9020133
U38	1	IC 74S64 AND-OR-INVERT	9010064
U39	1	IC 7438 QUAD 2-IN NAND	9000038
U40	1	IC 8303 8 BIT BUS DRIVER	8060303
U41-43	3	IC 74LS240 OCTAL BUFFER	9020240
VR1	1	REGULATOR 79L05 -5V	8051905

13/ Schematics





POWER SUPPLY SCHEMATIC DIAGRAM

14/Supplement

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