Radio Shack®

# TECHNICAL REFERENCE MANUAL

26-4921

# TRS-80® MODEL II

**Catalog Number 26-4921**

## Revised Floppy Disk Controller

SUPPLEMENT

CUSTOM MANUFACTURED IN U.S.A. BY RADIO SHACK A DIVISION OF TANDY CORPORATION

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## A. FUNCTIONAL SPECIFICATIONS

The Model II Floppy Disk Controller (FDC) Board has been redesigned to take advantage of a new chip set, the WD1691 and WD2143. This chip set provides more flexible write precompensation (continuously adjustable from 0 ns to 350 ns) and a simpler adjustment procedure for the data/clock recovery circuit.

The new design provides two independent drive interfaces, one for the internal drive and an additional interface for up to three external drives. This allows the system to start-up properly without damage to the system diskette even if the external drives are not turned on.

There is also no need for the disk terminator adaptor, currently required for single-drive systems. A provision to generate a software master reset to the WD1791 was also added (an OUT instruction to port E8H). This allows recovery from hang-up conditions which rarely occur in the WD179X family parts.

The redesigned FDC board is fully software compatible with the previous design, with the exception that an additional port is provided for the software master reset function. A redesign of the internal disk cable system is required, since there are now two independent drive interfaces. Field upgrades with redesigned FDC boards will also require the new cable system to be installed.

## B. THEORY OF OPERATION

### Decoding Logic

The FDC-PRINTER INTERFACE BOARD is an I/O (input-output) port map device which utilizes ports E0H, E1H, E2H, E3H, E4H, E5H, E6H, E7H, E8H and EFH.

**Table 1** summarizes the port allocation for the floppy controller board. Port-mapped devices use only the lower eight address bits to specify which port is being addressed.

The upper eight address bits are ignored completely and are not relevant to port-mapped devices. Three other signals (WR*, RD* and IOCY*) are used by port-mapped devices to determine whether an I/O operation is to occur. If WR* and IOCYC* are both low, this condition defines an output operation in progress.

**Figure 6** (FDC schematic diagram) should now be referred to for the remainder of the Decoding Logic discussion.

U21, pin 8, is the output of a four-input NAND gate. This pin should be low when any of the ports E0H through EFH are being addressed. U21, pin 6, is also an output of a four-input NAND gate which should go low when the port being addressed contains an F HEX in the low-order nibble of the port address.

**Table 1. Port Allocation**

| PORT # | ALLOCATION | FUNCTION |
|---|---|---|
| E0H | PIO Port A – Data | Printer and FDC INT. status |
| E1H | PIO Port B – Data | Printer Data (output) |
| E2H | PIO Port A – Control | Configuring Port A |
| E3H | PIO Port B – Control | Configuring Port B |
| E4H | FDC Status/CMD Register | FDC Status and CMD |
| E5H | FDC Track Register | Current Track Add. |
| E6H | FDC Sector Register | Current Sector Add. |
| E7H | FDC Data Register | Data To or From Diskette |
| E8H | Soft FDC Reset | Out Resets FDC |
| EFH | Drive Select Latch | Drive, Mode, Side Select |

These two outputs, labeled XF* and EX*, are combined at pins 4 and 5 of U22. U22, pin 6 is the decoder for the drive-select (U11) mapped at port EFH. This output is combined with OUT* at U22, pins 9 and 10 to produce the signal labeled DRVSEL* at U22, pin 8.

The rising edge of DRVSEL* is used by pin 9 of U11 to latch the data present on the internal data bus corresponding to an output to port EFH. This data pattern is used to determine the drive, mode, and side selection. The bit allocation for this latch is detailed in **Table 2**.

The signal labeled EX* is used as an enable to gate the addresses A3I and A2I to the control inputs of U23 (Binary to Decimal Decoder.) The signals A3I and A2I, along with A1I and A0I form the inputs to the decoder U23. U23, pins 1, 2, 3, 4, 5, 6, 7, 9 and 10 are the outputs which produce the chip enables for the PIO, FDC, and soft reset logic.

The port decode labeled E8* is combined with the signal OUT* at U34 pins 1 and 2. The resulting signal from U34 pin, 3 is combined with RESETI* at U14, pins 12 and 13. The output of U14, pin 11 is a low-going strobe which resets U18 if an output to port E8H is executed or the front-panel reset switch is actuated.

CPUIN is a signal generated by the decoding logic for the purpose of switching the direction of the data bus transceivers (U30, U31) in preparation for an input operation.

There are two conditions which require the data bus transceivers to switch direction such that they drive data outward to the system data bus:

(1) Port input operation
(2) Interrupt acknowledge cycle

The port-input operation is detected by the combination of any of the ports E0H through E7H being addressed concurrently with an input operation in progress.

U34, pin 11 will go low when this condition is detected. If SYNCI* and IORQI* are both low, this condition indicates an interrupt acknowledge cycle is in progress and that the interrupting device should present its vector to the data bus. Interrupt priority is determined by the signal IEIN (pin 13 of the system bus).

If IEIN is high during an interrupt acknowledge cycle, no device of higher priority is requesting service and the requesting device may bring its IEOUT low to prevent devices of lower priority from receiving service. A high on pin 1 of U5 indicates an interrupt acknowledge cycle is in progress. A high on pin 2 of U5 indicates no higher priority device is requesting service. A high on pin 13 of U5 indicates a device on this board is requesting service.

If all these conditions are true, pin 12, U5 (INTAK*) will go low. This output is combined with the output from pin 11 of U13 at pins 4 and 5 of U14. If either pin 4 or pin 5 of U14 goes low, then pin 6 of U14 will also go low. U2 inverts this signal and pin 12 of U2 will go high (CPUIN). If CPUIN is high, the data bus transceivers disable their receivers and enable their drivers to gate data onto the system data bus. This allows the PIO to transfer its interrupt vector to the CPU.

**Table 2. BIT Allocation**
**Port EFH, Drive Select Latch** (output only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Mode Select | Side Select | Unused | Unused | DRV3SEL | DRV2SEL | DRV1SEL | DRV0SEL |
| 0 = FM Mode | 0 = Side 1 | | | 1 = NOTSEL | 1 = NOTSEL | 1 = NOTSEL | 1 = NOTSEL |
| 1 = MFM Mode | 1 = Side 0 | | | 0 = SEL | 0 = SEL | 0 = SEL | 0 = SEL |

**NOTE**: D3 through D0 – only one of these bits should be low per output instruction.

### Bus Interface Logic

Good design practice dictates most signals to and from the system bus must be buffered so only one TTL load per board is presented to each non-inverting buffer for the Z-80 control signals. This buffering is accomplished by U32 and U33. (Note: The enables for both these parts are tied low, allowing these signals to be driven onto the board at all times. Open collector devices are used to drive the outputs to the bus which may be driven by other boards, INTRQ* and XFERRQ.)

There is a basic problem with using a Z-80/PIO with the WD1791. The PIO has a non-inverting data bus while the WD1791 utilizes an inverting data bus. One extra stage of inversion is required for the WD1791. U19 and U20 accomplish this extra inversion. These transceivers are normally receiving data but are enabled to drive data toward the system bus when an input operation from the ports assigned to the FDC is in progress.

### Z-80/PIO Interface Logic

The Z-80 parallel I/O (PIO) interface controller is a genera purpose, programmable, two-port device which provides TTL compatible interfacing between peripheral devices and the Z-80 CPU.

Any of the following modes can be selected for either port:

byte output
byte input
byte bi-directional A(port A only)
byte or control mode

In addition, the PIO provides a clean and minimal logic method for generating mode 2 interrupts to the Z-80 CPU.

Port A is used in the control mode, which allows the eight I/O lines (A0 through A7) to be configured as either inputs or outputs. An eight-bit mask register and a two-bit mask control register allow interrupts to be generated, dependent on the logic states of the I/O lines. Port A is primarily used for status checking and generating interrupts.

**Table 3. BIT Allocation**
**Port E0H, Printer, FDD, FDC Interrupt Status**

| D7 | D6 | D5 |
|---|---|---|
| Printer Busy | Paper Empty | Printer Select |
| 0 = Not Busy | 0 = Paper not Empty | 0 = Selected |
| 1 = Busy | 1 = Paper Empty | 1 = Not Selected |
| **D4** | **D3*** | **D2*** |
| Printer Fault | PRIME | Disk Change |
| 0 = Fault | High to Low | 0 = Door not Opened |
| 1 = Not Fault | Transition Resets Printer | 1 = Door Opened |
| **D1** | | **D0** |
| Two-Sided Diskette | | FDC INT REQUEST |
| 1 = Two-Sided Diskette Preset | | 1 = FDC is Interrupting |
| 0 = Single-Sided Diskette | | 0 = Not Interrupting |

*D2 indicates that the selected drive has had its door opened since it was last selected.

*D3 is an output which resets some printers.

One I/O line is configured as an output and provides the "prime" signal for the printer interface. The bit allocations for this port are detailed in **Table 3**.

Port B is used in the output mode for the purpose of outputting characters to the printer. The outputs of port B (B0 through B7) are isolated from the printer with an octal noninverting buffer, U4. (Note: The enables are tied low, gating whatever data is presented to the inputs of U4 directly to its outputs. The printer cable system routes this parallel data to the printer.)

Pin 21 of the PIO (U12), labeled BRDY, produces a high-going pulse which indicates valid data is present on the port B outputs. The rising edge of this pulse provides a trigger for pin 3 of U6. U6 is a one-shot which produces 1.5 μs low-going pulse at pin 4 when triggered.

The rising edge of the 1.5 μs strobe is used by the printer to latch the eight bits of parallel data present at the outputs of U4. The BRDY signal stays active until the rising edge of PACK* (which indicates the printer has accepted the data). The rising edge may also generate an interrupt if port B has been programmed to use interrupts. This provides an efficient method for determining when the printer can accept a new character without using status-checking loops.

The PIO interfaces directly to the system bus with a minimum of external components. D0 through D7 (U12) form a bi-directional data path to the system bus. The signals labeled A0l and A1l determine which port is addressed and whether the data transfer is intended for the command register.

If CEPIO*, IORQI*, and RDI* are all low, an input operation is in progress. If CEPIO* and IORQI* are low with RDI* high, an output operation is in progress. If IEIN is high, and INTRQI*, SYNCI*, IORQI* and IEO are low, an interrupt acknowledge cycle for the PIO is in progress. If SYNCI* is high and RESTI* is low, a low is produced at pin 8 of U14. If this sequence occurs without RDI* and IORQI* low, the PIO logic enters a reset state. For a more detailed discussion of the PIO operation, consult the *Zilog Z-80/PIO Technical Manual.*

### Disk Buss Selector Logic

The Model II Floppy Disk-Printer Interface Board supports up to four drives (one internal, three external). This function is implemented by using two disk-drive interface busses, one for the internal drive and one for the external drives. J0 is the connector used for the internal drive and P1 is the edge connector used for the external drives.

U17 and U16 (quad two-to-one data selectors) are used to select which set of inputs from the disk drive busses are routed to the 1791 FDC chip. Pin 1 of both parts are the control pins for the data selector. If U17, pin 1 and U16, pin 1 are high, the external inputs are selected. A low selects the internal inputs.

This control signal (labeled INT*/EXT) is derived from the outputs of a decimal decoder (U36). U36 uses the lower four bits of the drive-select latch (U11) as its inputs to decode which drive is selected. The decoder used in this way prevents more than one drive from being selected at a time.

### Read/Write Data Pulse Shaping Logic

Two one-shots (1/2 of U15 and 1/2 of U6) are used to ensure the read and write data pulses are approximately 250 ns in duration.

### Disk Buss Output Drivers

U25 and U10 are high-current open collector drivers used to buffer the output signals from the drive select latch and the FDC chip to the floppy disk drives. (Schematic note: Each output signal to the drives has two buffers associated with each signal — one set is used for the internal drive buss and the other set is used for the external drive buss. No select logic is required for these output signals since the drive select bits define which drive is active.)

### Write Precompensation and Clock Recovery Logic

U28 (WD1691), U29 (WD2143) and U24 (LS629), along with a few passive components, comprise the write precompensation and read clock recovery logic.

The WD1691 is an LSI device which minimizes the external logic required to interface the 1791 FDC chip to a disk drive. With the use of an external VCO (U24), the WD1691 will derive the RCLK signal for the 1791, while providing an adjustment signal for the VCO, to keep the RCLK synchronous with the read data from the drive.

Write precompensation control signals are also provided by the WD1691 to interface directly to the WD2143 (U29) clock generator.

The read clock recovery section of the WD1691 has five inputs: $\overline{\text{DDEN}}$, VCO, RDD*, WG and VFOE*; and three outputs: PU, PD* and RCLK. The inputs VFOE* and WG, when both low, enable the clock recovery logic. When WG is high, a write operation is in progress and the clock recovery circuits are disabled regardless of the state of any other inputs.

The write precompensation section of the WD1691 was designed to be used with the WD2143 clock generator. Write precompensation is not used in single-density mode and the signal $\overline{\text{DDEN}}$ when high indicates this condition.

In double-density mode ($\overline{DDEN}$ = Ø), the signals EARLY and LATE are used to select a phase input (Ø1*-Ø4*) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143 to start its pulse generation. Ø2* is used as the write data pulse on nominal (EARLY = LATE = Ø), 01* is used for the early and Ø3* is used for the late. The leading edge of 04* resets the STB line in anticipation of the next data pulse. When TG43 = Ø or $\overline{DDEN}$ = 1, precompensation is disabled and any transitions on the WDIN line will appear on the WDOUT line.

When VFOE* and WG are low, the clock recovery circuits are enabled. When the RDD* line goes low, the PU or PD* signals will become active.

If the RDD* line has made its transition in the beginning of the RCLK window, PU will go from a high impedance state to a logic one, requesting an increase in VCO frequency. If the RDD* line has made its transition at the end of the RCLK window, PU will remain in the high impedance state while PD* will go to a logic zero, requesting a decrease in the VCO frequency.

When the leading edge of RDD* occurs in the center of the RCLK window, both PU and PD* will remain in the high impedance state, indicating that no adjustment of the VCO frequency is required. By tying PU and PD* together, an adjustment signal is created which will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency.

To speed up rise times and stabilize the output voltage, a resistor divider, using R2, R21 and R24, is used to adjust the tri-state level at approximately 1.4V. This adjustment results in a worst case voltage swing of +/−1V, which is acceptable for the frequency control input of the VCO (U24).

This signal derived from the combination of PU and PD* will eventually correct the VCO input to exactly the same frequency multiple as the RDD* signal. The leading edge of the RDD* signal will then occur in the exact center of the RCLK window, an ideal condition for the 1791 internal recovery circuits.

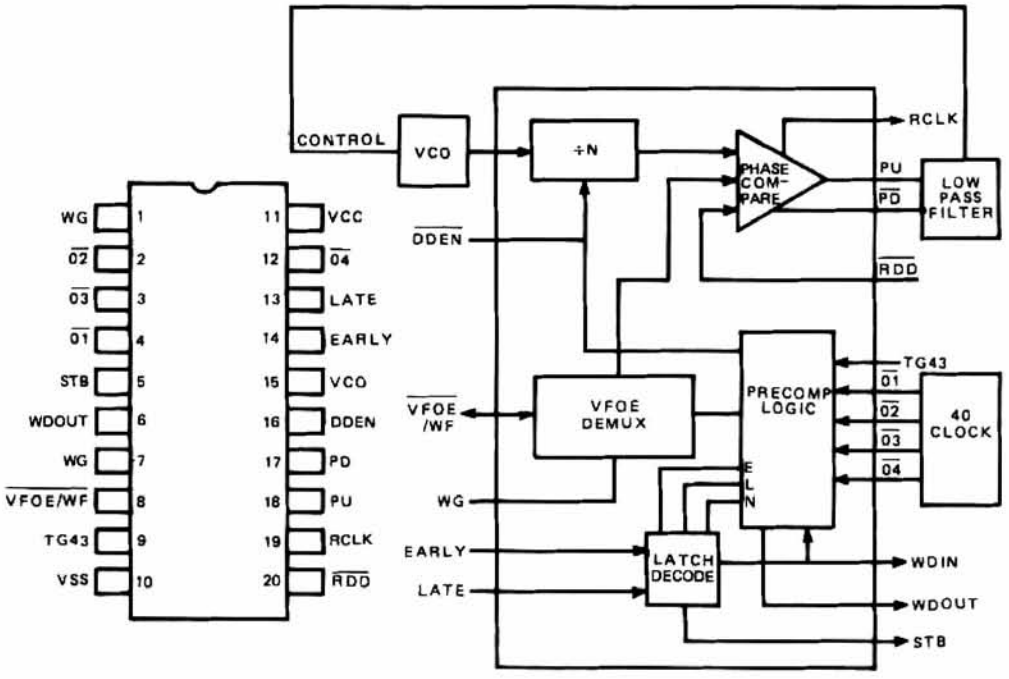



**Figure 1. WD1691 Block Diagram**

### WD1791 — Floppy Disk Controller IC

The WD1791 is an MOS LSI device which performs the functions of a Floppy Disk format/controller in a single-chip implementation.

The WD1791 contains all the features of its predecessor, the 1771, plus the added features necessary to read, write and format a double-density diskette. These include: address mark detection, FM and MFM encode and decode logic, window extension and write precompensation.

### WD1791 Organization

The Floppy Disk Formatter block diagram is illustrated in Figure 2. The primary sections include the parallel Processor Interface and the Floppy Disk interface.

**Data Shift Register** — This eight-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

**Data Register** — This eight-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command, the Data Register holds the address of the desired track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

**Track Register** — This eight-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards Track 76) and decremented by one when the head is stepped out (towards Track 0). The contents of the register are compared with the record track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the FDC is busy.

**Sector Register (SR)** — This eight-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the

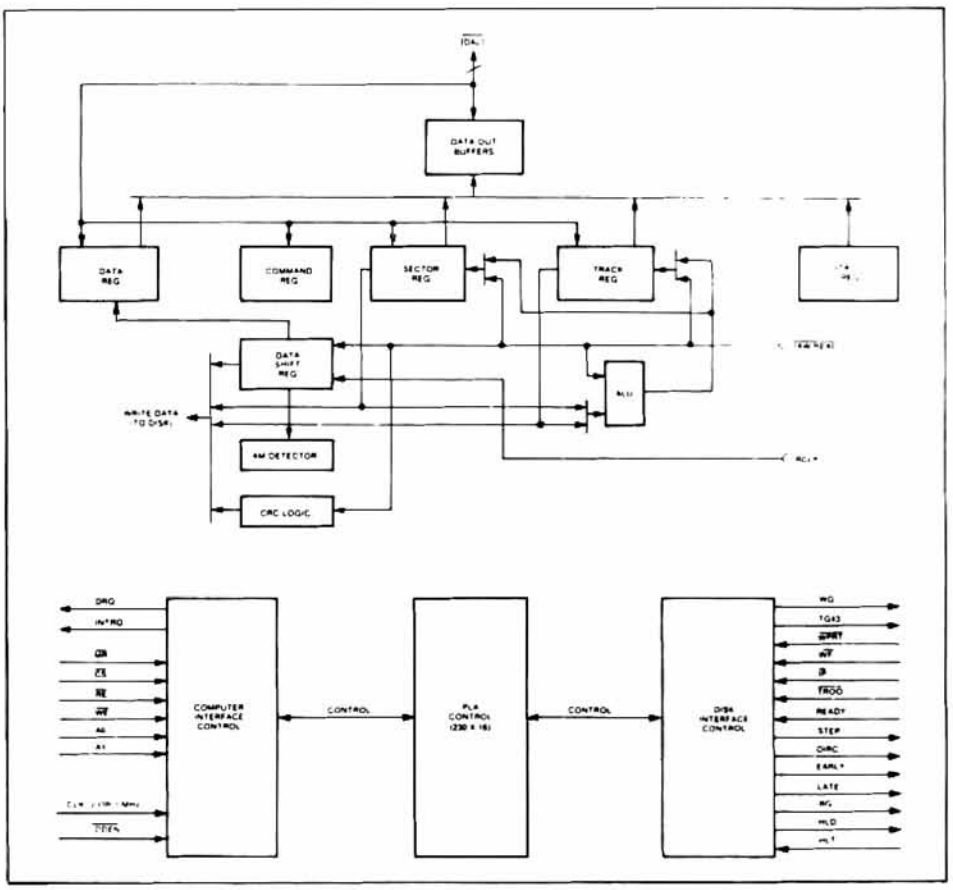



**Figure 2. WD1791 Block Diagram**

ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the FDC is busy.

**Command Register (CR)** — This eight-bit register holds the command presently being executed. This register should not be loaded when the FDC is busy except to load a force interrupt command. This action results in an interrupt. The command register can be loaded from the DAL but not read onto the DAL.

**Status Register (STR)** — This eight-bit register holds device Status information. The meaning of the Status bits is a function of the contents of the Command Register. This register can be read onto the DAL but not loaded from the DAL.

**CRC Logic** — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is present to ones (1's) prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)** — The ALU is a serial comparator, incrementor and decrementor. It is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control** — All computer and Floppy Disk interface controls are generated throughout the logic. The internal device timing is generated from an external clock.

The 1791 has two different modes of operation, according to the state of $\overline{DDEN}$. When $\overline{DDEN} = 0$, double density (MFM) is assumed. When $\overline{DDEN} = 1$, single density (FM) is assumed.

**AM Detector** — This address mark detector detects ID, data and index address marks during Read and Write operations.

**Processor Interface**

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status and Control word out of, or into, the FD1791.

The DAL are three-state buffers that are enabled as output drivers when Chip Enable (CE*) and Read Enable (RE*) are active (low-logic state) or act as input receivers when CE* and Write Enable (WE*) are active.

When transfer of data to the Floppy Disk Controller is required by the host processor, the device address is decoded and CE* is made low. The least-significant address bits A1 and A0, combined with the signals RE* during a Read operation or WE* during a Write operation, are interpreted as selecting the following registers:

| Port Address | A1-A0 | | Read (RE*) | Write (WE*) |
|---|---|---|---|---|
| | A1 | A0 | | |
| E4H | 0 | 0 | Status Register | Command Register |
| E5H | 0 | 1 | Track Register | Track Register |
| E6H | 1 | 0 | Sector Register | Sector Register |
| E7H | 1 | 1 | Data Register | Data Register |

**Table 4. Register Sheet**

During Direct Memory Access (DMA), types of data transfers between the Data Register of the FD1791 and the DMA, the Data Request (DRQ) output is used in data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operation, the Data Request is activated (set high when an assembled serial input byte is transferred in parallel to the Data Register). This bit is cleared when the Data Register is read by the processor or DMA controller.

If the Data Register is read after one or more characters are lost (by having new data transferred into the register prior to the processor readout), the Lost Data bit is set in the Status Register. The Read operation continues until the end of the sector is reached.

On Disk Write operations, the Data Request is activated when the Data Register transfers its contents to the Data Shift Register and requires a new data byte. It is reset when the Data Shift Register is loaded with new data by the processor or DMA controller.

If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command, an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated when a Force Interrupt command condition is met.

**Floppy Disk Interface**

The WD1791 has two modes of operation, according to the state of DDEN (pin 37). When DDEN = 1, single density is selected. When DDEN = Ø, double density is selected. In either case, the CLK input (pin 24) is at 2 MHz. When the clock is at 2MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable if TEST* = 1.

**Head Positioning**

Four commands cause positioning of the Read-Write head (refer to the FDI 79X-C2 Data Sheet published by Western Digital.) The period of each positioning step is specified by the r field in bits 1 and Ø of the command word.

After the last directional step, an additional 15 milliseconds (ms) of head-setting time takes place if the Verify flag is set in Type I commands. (Note: This time doubles to 30 ms for a 1 MHz clock.) If TEST = Ø, there is zero-setting time. There is also a 15ms head-setting time if the E flag is set in any Type II or III command.

The rates (shown in **Table 5**) can be applied to a Step-Direction Motor through the device interface.

**Step** — A 2μs (MFM) or 4μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the directional output.

**Direction (DIRC)** — The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1.

The verification operation begins at the end of the 15μs setting time after the head is loaded against the media. The track number for the first encountered ID Field is compared against the contents of the Track Register.

If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The 1791 must find an ID field with a correct track number and a correct CRC within five revolutions of the media; otherwise, the seek error is set and an INTRQ is generated.

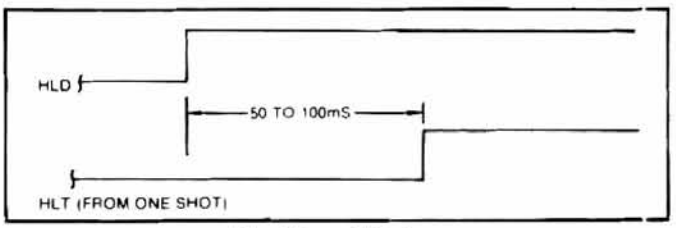
The following example explains the use of the Stepping Rates Table: If Clock is 2MHz and DDEN (double density not) is high (1) and if bit R1 is low (Ø) while bit R0 is high (1) and TEST is high (1), then the stepping time will be six ms/step.

| CLK | 2MHz | 2MHz | 1MHz | 1MHz | 2MHz | 1MHz |
|---|---|---|---|---|---|---|
| DDEN | Ø | 1 | Ø | 1 | X | X |
| R1R0 | TEST =1 | TEST =1 | TEST =1 | TEST =1 | TEST =Ø | TEST =Ø |
| Ø Ø | 3 ms | 3 ms | 6 ms | 6 ms | Approx. | Approx. |
| Ø 1 | 6 ms | 6 ms | 12 ms | 12 ms | 200μS | 400μS |
| 1 Ø | 10 ms | 10 ms | 20 ms | 20 ms | | |
| 1 1 | 15 ms | 15 ms | 30 ms | 30 ms | | |

**Table 5. Stepping Rates**

The Head Load (HLD) output controls the movement of the Read/Write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag is set (V = 1), or upon receipt of any Type II or III command. Once HLD is active, it remains active until either a Type I command is received with (h = Ø and V = Ø); or if the FD1791 is an idle state (non-busy) and 15 index pulses have occurred, it is reset.

Head Load Timing (HLT) is an input to the FD1791 which is used for the head engage time. When HLT = 1, the FD1791 assumes the head is completely engaged. The head engage time is typically 30 to 65 ms, depending on the specifications of the drive used.




**Head Load Timing**

The low to high transition on HLD is used to fire a one shot (1/2 of U15). This one shot has a time period of approximately 50ms. The output of the one shot is then used for HLT and supplied as an input to the 1791.

When both HLD and HLT are true, the 1791 will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: If h = Ø and V = Ø, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15ms delay. If h = Ø and V = 1, HLD is set near the end of the command, an internal 15ms delay occurs, and the FD1791 waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command.

Near the end of the command, after all the steps have been issued, an internal 15ms delay occurs and the 1791 then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15ms delay occurs and then HLT is sampled until true.

**Disk Read Operations**

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical 1. For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical 0.

Sector lengths are determined at format time by a special byte in the ID field. If this Sector Length byte in the ID field is zero, then the sector length is 128 bytes. If 01, then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes.

The number of sectors per track, as far as the 1791 is concerned, can be from 1 to 255 sectors. The number of tracks, as far as the 1791 is concerned, is from 0 to 255 tracks.

For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with eight sectors/track.

For read operation, the FD1791 request a $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition (at 2 MHz clock) and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by a phase-locked loop or counter techniques.

In addition, a Read Gate Signal is provided as an output (Pin 25) which informs some phase-locked loops when to acquire synchronization. However, pin 25 is not used in this design.

**Disk Write Operations**

When writing is to take place on the diskette, the Write Gate (WG) output is activated. This allows current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the 1791 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case, any Write command is immediately terminated, an interrupt is generated, and the $\overline{\text{Write Protect}}$ status bit is set.

The Write Fault input, when activated, signifies a writing fault condition detected in disk-drive electronics such as failure to detect Write current flow when the Write Gate is activated. On detection of this fault, the FD1791 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For Write operation, the WD1791 provides a Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write Data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0) for 1 MHz clock. Write Data provides the unique address marks in both formats.

Also during Write, two additional signals are provided for Write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. EARLY is valid for the duration of the pulse. LATE is active true when the WD pulse is to be written late. If both are low when a WD pulse is present, the WD is written at nominal.

The Write precompensation signals EARLY and LATE are valid in both FM and MFM formats. However, the 1691 will ignore these signals unless TG 43 and $\overline{\text{DDEN}}$ are both active.

Whenever a Read or Write command (Type II or III) is received, the FD1791 samples the Ready input. If this input is logic low, the command is not executed and an interrupt is generated. This also applies to Type I commands.

**Recording Codes**

Information is stored on a disk using a code that takes the desired information and converts it to a pulse that the recording system can write and recover from the disk. The ideal system requires that all the pulses written on the disk be informational

The problem with this type of system is when the data is recovered, it is not self-clocking. Self-clocking codes include Frequency Modulation (FM) and Modified Modulation (MFM). The actual flux reversal rate of the two codes is the same; **Table 6** shows the differences.

**Frequency Modulation (FM):** Information is always recorded by inserting a clock between each data bit. A "1" bit is defined as a flux transition between clocks while a "Ø" is defined as the absence of this flux transition. Clocks are always flux transition.

**Modified Frequency Modulation (MFM):** Information is encoded using data and clocks. The longest time between flux transitions is the same as the FM code but clocks are not recorded between data bits.

**Definitions:**

1. "1" is defined as a flux transition occurring at the half-cell time.

2. "Ø" is defined as a flux transition occurring at the start of the cell time. A pulse at the beginning of the cell is a clock; however, a clock is not always written. Clock is suppressed if there is a "1" in this cell or if there was a "1" in the preceding cell.

**Table 6. Self-Clocking Codes**

| | DOUBLE FREQUENCY | MODIFIED FREQUENCY MODULATION |
|---|---|---|
| Bit Density | 1836<br>3268 | 3672 (outer track)<br>6536 (inner track) |
| Data Transfer Rate | 249,984 Hz | 499,968 Hz |
| Bits/Track | 42,664 | 83,328 |
| Bits/Disk | 3,2Ø8,128 | 6,416,256 |
| Cell Time | 4µs | 2µs |
| Flux Density (inner track) | 6536 | 6536 |

### Adjustments and Jumper Options

The data separator must be adjusted with the 1791 in an idle condition (no command currently in operation). Adjust R2 potentiometer for a 1.4V level on test point 25. Then adjust R1 potentiometer to yield a 4MHz square wave at pin 16 of U28.

The write precompensation must be adjusted while executing a continuous-write command (Example: Format). Adjust R3 potentiometer to yield 250-ns-wide pulses at test point 27. This results in a write precompensation value of 25Ø ns.

There are a number of jumper options available on a controller board. (**Table 7**) describes the standard configuration as normally used by the Model II system.

**Standard Configuration**

| Installed Jumpers | Function |
|---|---|
| B to C | 8-inch drive ready signal |
| J to K | EØH-EFH port addressing |
| L to M | active high XFERRQ |
| P to Q | 2-MHz FDC clock |
| T to U | drive Ø INT*/EXT select |

**Optional Configuration**

| Installed Jumpers | Function |
|---|---|
| D to E | prime signal to printer |
| Q to R | 1 MHz FDC clock |
| M to N | active low XFERRQ |
| I to J | AØH-AFH port addressing |
| A to B | mini-drive ready signal |
| H to F, S to T | Two internal mini-drives INT*/EXT select |

**Table 7. Adjustment Table**

## J1 (FDC Board to Floppy Disk) SIGNAL DESCRIPTIONS

| PIN | SIGNAL NAME | DESCRIPTION |
|---|---|---|
| 1 | GND | Power Ground |
| 2 | WRTCRT* | Reduced Write Current |
| 3 | GND | Power Ground |
| 4 | NC | Not Connected |
| 5 | GND | Power Ground |
| 6 | NC | Not Connected |
| 7 | GND | Power Ground |
| 8 | NC | Not Connected |
| 9 | GND | Power Ground |
| 10 | TWOSID* | Two Sided Diskette Installed |
| 11 | GND | Power Ground |
| 12 | DSKCHG* | Drive Door Opened Since Last Select |
| 13 | GND | Power Ground |
| 14 | SDSEL | Side Select: low = side Ø , high = side 1 |
| 15 | GND | Power Ground |
| 16 | NC | Not Connected |
| 17 | GND | Power Ground |
| 18 | HLD* | Head Load |
| 19 | GND | Power Ground |
| 20 | IP* | Index Pulse |
| 21 | GND | Power Ground |
| 22 | RDY | Drive Ready |
| 23 | GND | Power Ground |
| 24 | NC | Not Connected |
| 25 | GND | Power Ground |
| 26 | DS1* | Drive Select One |
| 27 | GND | Power Ground |
| 28 | DS2* | Drive Select Two |
| 29 | GND | Power Ground |
| 30 | DS3* | Drive Select Three |
| 31 | GND | Power Ground |
| 32 | DS4* | Drive Select Four |
| 33 | GND | Power Ground |
| 34 | DIR* | Step Direction |
| 35 | GND | Power Ground |
| 36 | STEP* | Step Head One Track |
| 37 | GND | Power Ground |
| 38 | CPWD* | Write Data |
| 39 | GND | Power Ground |
| 40 | WG* | Write Gate |
| 41 | GND | Power Ground |
| 42 | TRKØ* | Track Zero Indication |
| 43 | GND | Power Ground |
| 44 | WPRT* | Write Protected Diskette |
| 45 | GND | Power Ground |
| 46 | RD* | Read Data |
| 47 | GND | Power Ground |
| 48 | NC | Not Connected |
| 49 | GND | Power Ground |
| 50 | NC | Not Connected |

*Indicates an inverted signal or an active low signal.

## J2 (FDC Board to Line Printer) SIGNAL DESCRIPTIONS

| PIN | SIGNAL NAME | DESCRIPTION |
|---|---|---|
| 1 | PSTB* | Data Strobe |
| 2 | GND | Power Ground |
| 3 | PDAT Ø | Data Bit Ø to Printer |
| 4 | GND | Power Ground |
| 5 | PDAT 1 | Data Bit 1 to Printer |
| 6 | GND | Power Ground |
| 7 | PDAT 2 | Data Bit 2 to Printer |
| 8 | GND | Power Ground |
| 9 | PDAT 3 | Data Bit 3 to Printer |
| 10 | GND | Power Ground |
| 11 | PDAT 4 | Data Bit 4 to Printer |
| 12 | GND | Power Ground |
| 13 | PDAT 5 | Data Bit 5 to Printer |
| 14 | GND | Power Ground |
| 15 | PDAT 6 | Data Bit 6 to Printer |
| 16 | GND | Power Ground |
| 17 | PDAT 7 | Data Bit 7 to Printer |
| 18 | GND | Power Ground |
| 19 | PACK* | Printer Data Acknowledge |
| 20 | GND | Power Ground |
| 21 | BUSY | Printer Busy |
| 22 | GND | Power Ground |
| 23 | PE | Paper Empty |
| 24 | GND | Power Ground |
| 25 | PSEL | Printer Selected |
| 26 | PRIME | Printer Reset |
| 27 | GND | Power Ground |
| 28 | FAULT | Printer Fault |
| 29 | NC | Not Connected |
| 30 | NC | Not Connected |
| 31 | GND | Power Ground |
| 32 | NC | Not Connected |
| 33 | GND | Power Ground |
| 34 | NC | Not Connected |

*Indicates an inverted signal or an active low signal.

## FLOPPY DISK CONTROLLER PARTS LIST

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---|---|---|---|
| | ELECTRICAL | | |
| | PC Board | 8709198 | |
| | FDC PC Board Assembly | 8893658 | |
| | Cable, FDC to Rear Panel | 8702217 | |
| | Cable, FDC to Internal Diskette | 8702216 | |
| | CAPACITORS | | |
| C1-2 | Capacitor 0.1μF 50V +80-20% Z5U | 8384104 | ACC104QJAP |
| C3 | Capacitor 200PF 50V C. Disk 5% NPO | 8301203 | |
| C4 | Capacitor 47pF 50V Disk 5% NPO | 8300203 | |
| C5-8 | Capacitor 0.1μF 50V +80-20% Z5U | 8384104 | ACC104QJAP |
| C9 | Capacitor 47pF 50V C. Disk 5% NPO9 | 8300203 | |
| C10 | Capacitor .1μF 50V +80-20% Z5U | 8384104 | ACC104QJAP |
| C11 | Capacitor 0.68μF 50V C. Disk 10% | 8304684 | |
| C13-20 | Capacitor 0.1μF 50V +80-20% Z5U | 8384104 | ACC104QJAP |
| C21 | Capacitor 20PFD 50V C. Disk 5% NPO | 8300473 | |
| | Jumper Plugs | 8519021 | AJ6769 |
| C22 | Capacitor 33μF 16V Electrical Radial | 8396331 | |
| C23 | Capacitor 0.33μF 100V 10% POLY | 8354335 | |
| C24 | Capacitor 0.1μF 50V +80-20% Z5U | 8384104 | ACC104QJAP |
| C25 | Capacitor 33UF 16V Electrical Radial | 8396331 | |
| | DIODES | | |
| CR1 | Diode Zener SZG30368RL | 8150682 | ADX1518 |
| | RESISTORS | | |
| R1 | Trim Pot 50K ohm .155 Watt | 8279350 | AP7168 |
| R2 | Trim Pot 100K ohm .155 Watt | 8279410 | |
| R3 | Trim Pot 10K ohm .155 Watt | 8279310 | |
| R4-5 | Resistor 2.2K ohm 1/4 Watt 5% | 8207222 | ANO216EEC |
| R6-8 | Resistor 4.7K ohm 1/4 Watt 5% | 8207247 | ANO247EEC |
| R9 | Resistor 8.2K ohm 1/4 Watt 5% | 8207282 | ANO271EEC |
| R10 | Resistor 20K ohm 1/4 Watt 5% | 8207320 | ANO306EEC |
| R11 | Resistor 8.2K ohm 1/4 Watt 5% | 8207282 | ANO271EEC |
| R12-14 | Resistor 2.2K ohm 1/4 Watt 5% | 8207222 | ANO216EEC |

| | | | |
|---|---|---|---|
| R15 | Resistor 10K ohm 1/4 Watt 5% | 8207310 | ANO281EEC |
| R16 | Resistor 4.7K ohm 1/4 Watt 5% | 8207247 | ANO247EEC |
| R17-18 | Resistor Pak 150 ohm (8-pin sip) | 8290016 | |
| R19-20 | Resistor 2.2K ohm 1/4 Watt 5% | 8207222 | ANO216EEC |
| R21 | Resistor 47K ohm 1/4 Watt 5% | 8207347 | ANO340EEC |
| R22 | Resistor 150 ohm 1/4 Watt 5% | 8207115 | ANO142EEC |
| R23 | Resistor 390K ohm 1/4 Watt 5% | 8207439 | ANO414EEC |
| R24 | Resistor 47K ohm 1/4 Watt 5% | 8207347 | ANO340EEC |
| R25-26 | Resistor 4.7K ohm 1/4 Watt 5% | 8207247 | ANO247EEC |
| R27 | Resistor 330 ohm 1/4 Watt 5% | 8207133 | ANO159EEC |
| R28-29 | Resistor 10K ohm 1/4 Watt 5% | 8207310 | ANO281EEC |
| R30-31 | Resistor 4.7K ohm 1/4 Watt 5% | 8207247 | ANO247EEC |
| R32 | Resistor 33 ohm 1/4 Watt 5% | 8207033 | ANOO87EEC |
| R33 | Resistor 4.7K ohm 1/4 Watt 5% | 8207247 | ANO247EEC |
| R34 | Resistor Pak 150 ohm (8-pin sip) | 8290016 | |
| R35 | Resistor 4.7K ohm 1/4 Watt 5% | 8207247 | ANO247EEC |
| R36 | Resistor 2.2K ohm 1/4 Watt 5% | 8207222 | ANO216EE |
| R37 | Resistor 10K ohm 1/4 Watt 5% | 8207310 | ANO281EEC |

CIRCUITS

| | | | |
|---|---|---|---|
| U1 | IC 74LS20 Dual 4-In Nand | 9020020 | AMX3555 |
| U2-3 | IC 74LS04 Hex Inverter | 9020004 | AMX3552 |
| U4 | IC 74LS244 Octal 3-State Driver | 9020244 | AMX3864 |
| U5 | IC 74LS10 Triple 3-In Nand | 9020010 | AMX3898 |
| U6 | IC 74LS123 Multivibrator 4-in NOR | 9020123 | AMX3803 |
| U7 | IC 7416 Hex Inverter Open-C | 9000016 | |
| U9 | IC 74LS367 Hex 3-State Driver | 9020367 | AMX3567 |
| U10 | IC 7407 Hex Buffer Open-C | 9000007 | |
| U11 | IC 74LS174 Hex D-Flip Flop | 9020174 | AMX3565 |
| U12 | IC Z80-PIO Parallel I/O Control | 8047881 | AXX3015 |
| U13 | IC 74LS32 Quad 2-In Or | 9020032 | AMX3557 |
| U14 | IC 74LS08 Quad 2-In AND | 9020008 | AMX3698 |
| U15 | IC 74LS123 Multivibrator | 9020123 | AMX3803 |
| U16 | IC 74LS158 Quad 2-In Mux Invert | 9020157 | |
| U17 | IC 74LS158 Quad 2-In Mux | 9020157 | |
| U18 | IC WD1791-02 Floppy Formatter | 8045791 | AXX3014 |
| U19-20 | IC 8T26A Quad Buss Transceiver | 9060026 | AMX4261 |
| U21 | IC 74LS20 Dual 4-In NAND | 9020020 | AMX3555 |
| U22 | IC 74LS32 Quad 2-In OR | 9020032 | AMX3557 |
| U23 | IC 74LS145 1 of 10 Decoder | 9020042 | AMX4659 |
| U24 | IC 74LS629 VCO | 9020629 | AMX4663 |
| U25 | IC 7416 Hex Inverter Open-C | 9000016 | |
| U26 | IC 74LS74 D-Flip Flop | 9020074 | AMX3558 |
| U27 | IC 7407 Hex Buffer Open-C | 9000007 | |
| U28 | IC WD1691 Floppy Support Logic | 8040691 | |
| U29 | IC WD2143-01 4-Phase Clock | 8040143 | |
| U30-31 | IC 8T26A Quad Buss Transceiver | 9060026 | AMX4261 |
| U32 | IC 74LS240 Octal Inverting Driver | 9020240 | AMX4225 |
| U33 | IC 74LS367 Hex 3-State Buffer | 9020367 | AMX3567 |
| U34 | IC 74LS32 Quad 2-In OR | 9020032 | AMX3557 |
| U35 | IC 74LS74 D-Flip Flop | 9020074 | AMX3558 |
| U36 | IC 74LS42 1 of 10 Decoder | 9020145 | |
| U37-38 | IC 74LS04 Hex Inverter | 9020004 | AMX3552 |

REGULATOR

| | | | |
|---|---|---|---|
| VR1 | Regulator MC78L05AC | 8052805 | |

## MISCELLANEOUS

| | | | |
|---|---|---|---|
| J0 | Connector 50-Pin PC Mount | 8519117 | |
| J1-2 | Connector 34-pin PC Mount | | |
| | Socket 40-Pin Dip | 8509002 | AJ6580 |
| | Socket 20-Pin Dip | 8509009 | AJ6760 |
| | Socket 18-Pin Dip | 8509006 | AJ6701 |
| | Staking Pin | 8529014 | AHB9682 |

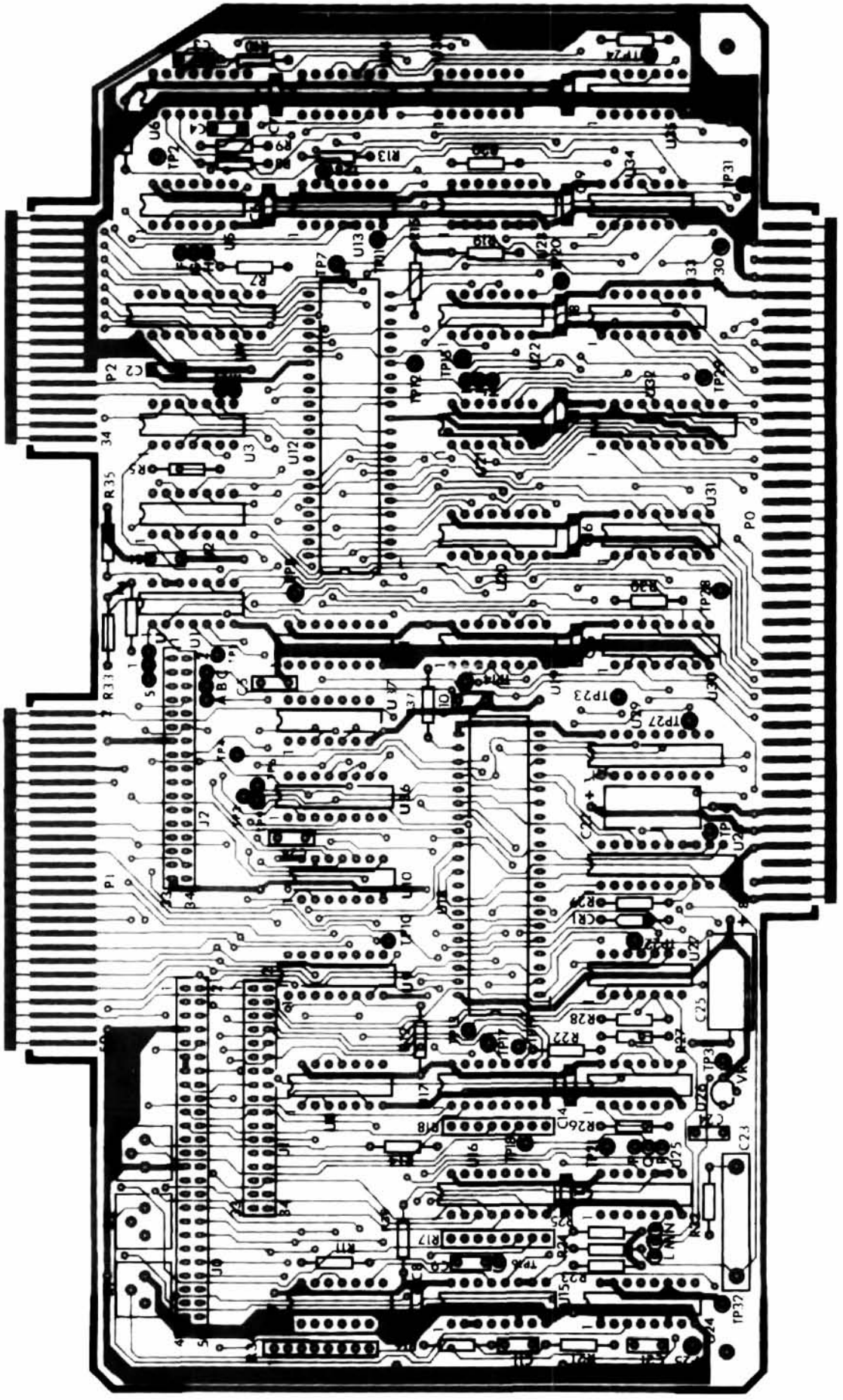


Figure 4. X-Ray View FDC Printed Circuit Board — Component Side

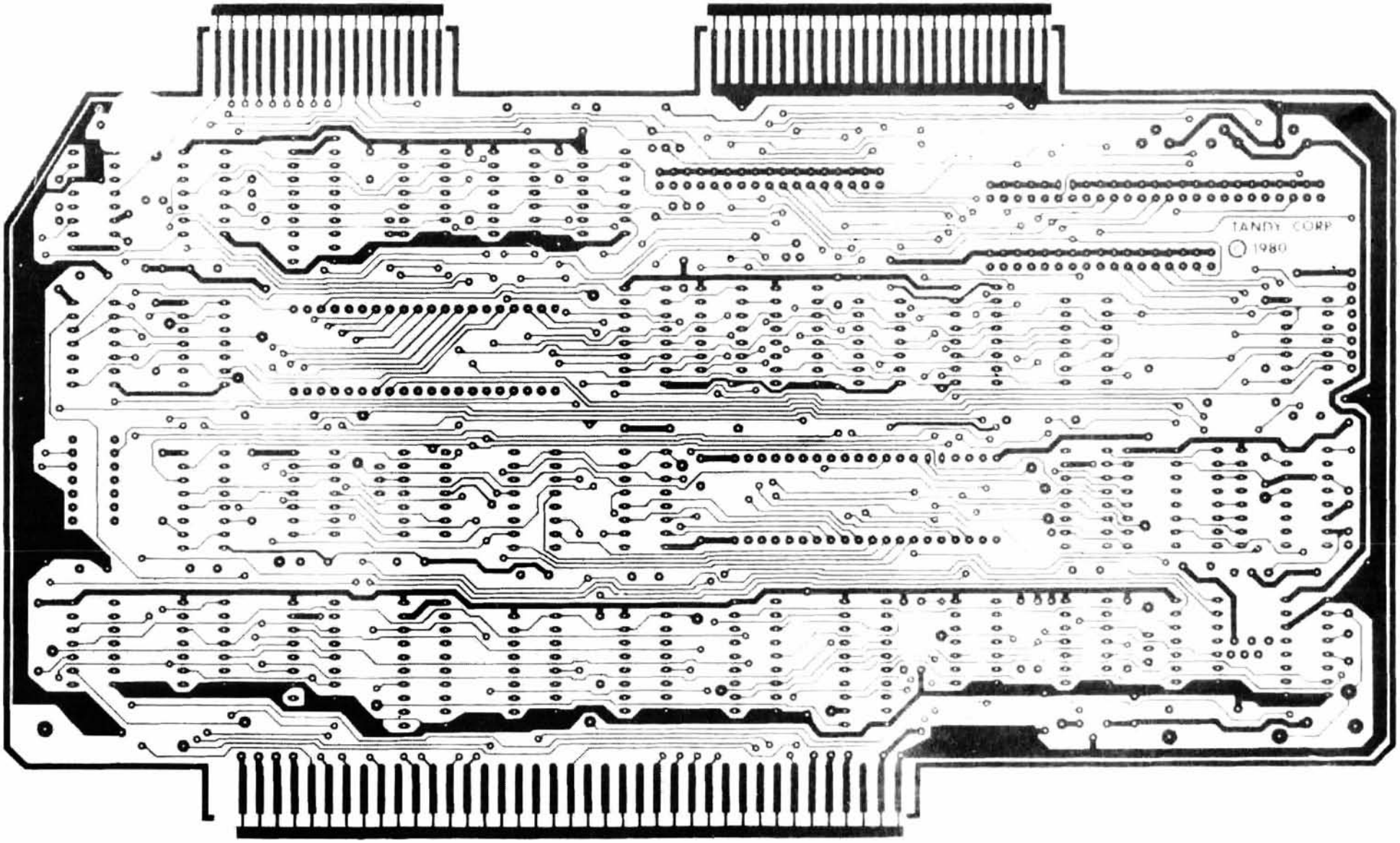



**Figure 5. X-Ray View FDC Printed Circuit Board — Circuit Side**

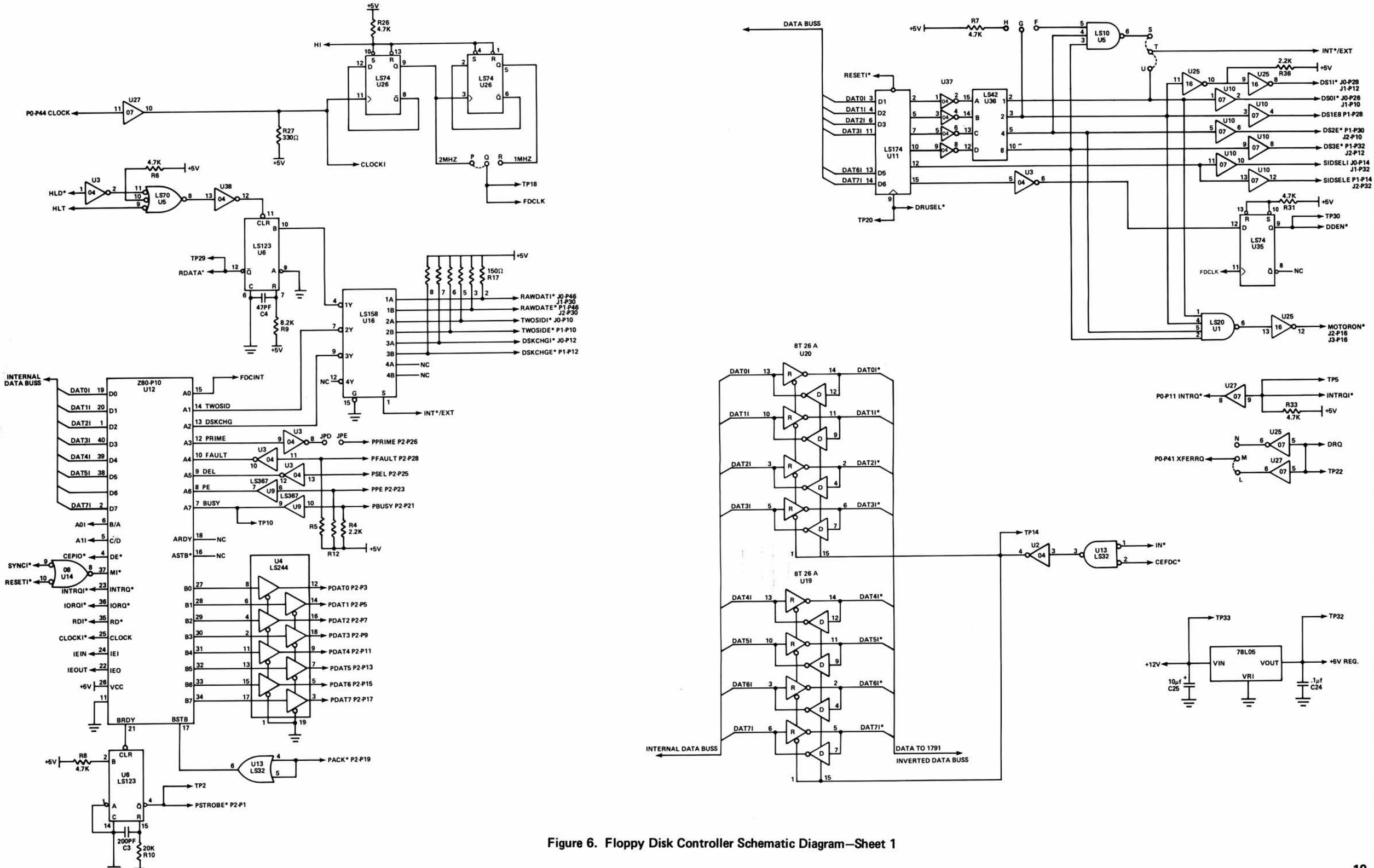



**Figure 6. Floppy Disk Controller Schematic Diagram—Sheet 1**

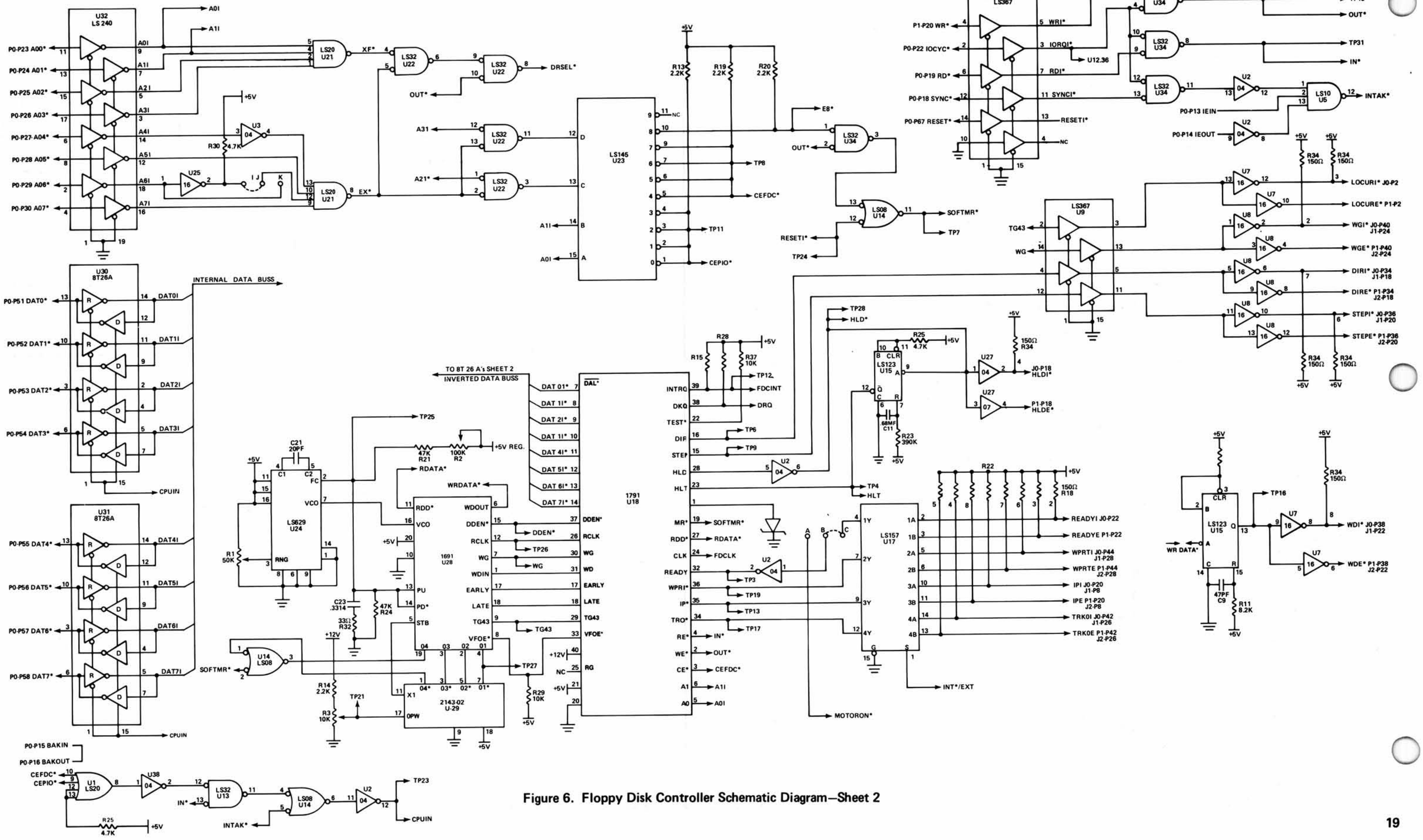



**Figure 6. Floppy Disk Controller Schematic Diagram—Sheet 2**

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